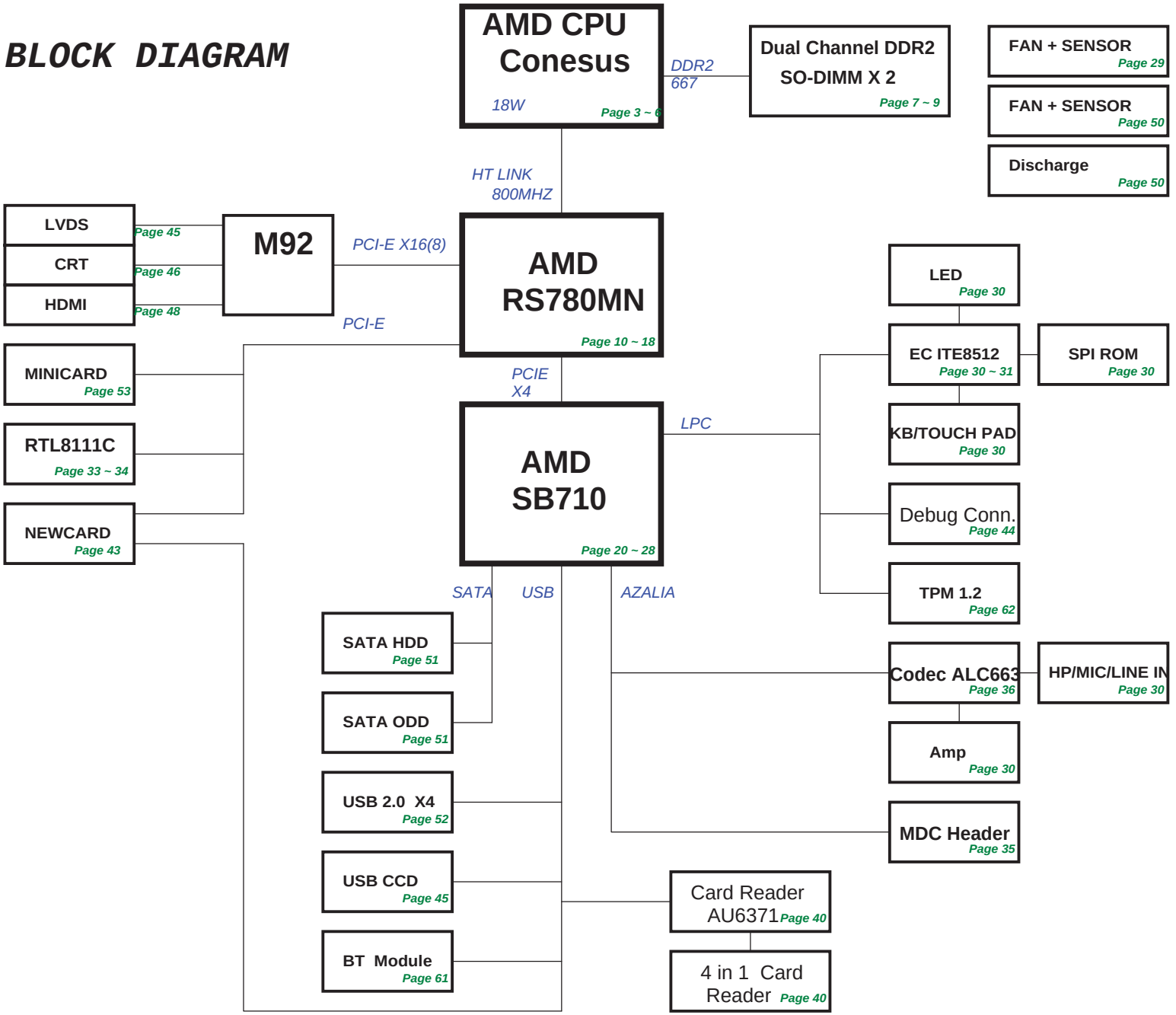
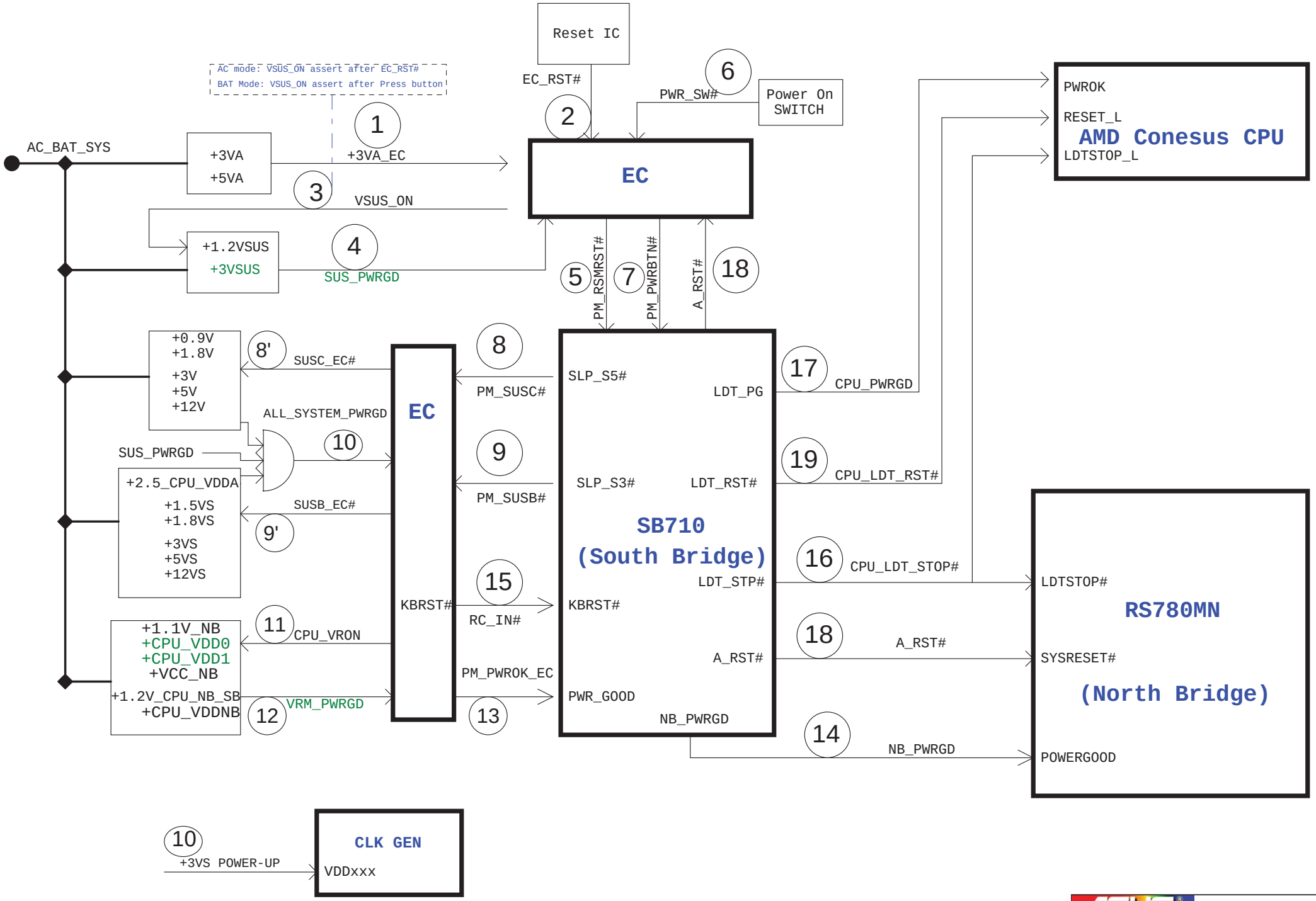
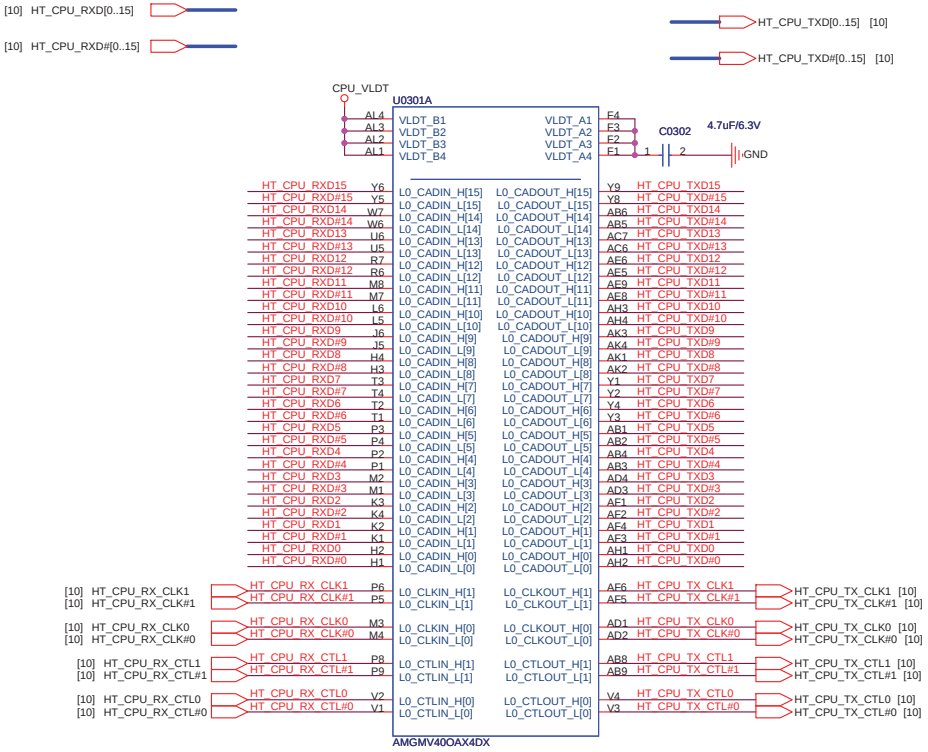
BLOCK DIAGRAM



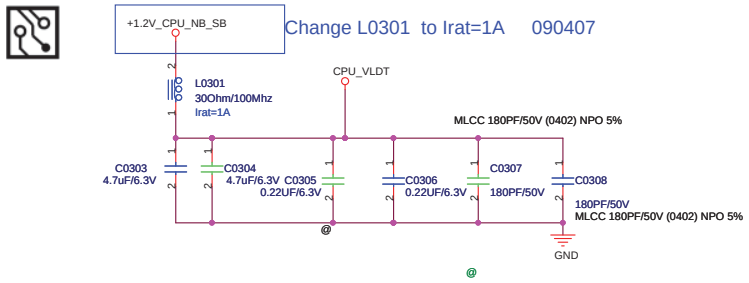
ASUSTeK Computer INC	Title : Block Diagram	
	Engineer: Ice_wang	
Size: Custom	Project Name: F83T	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 1 of 91	



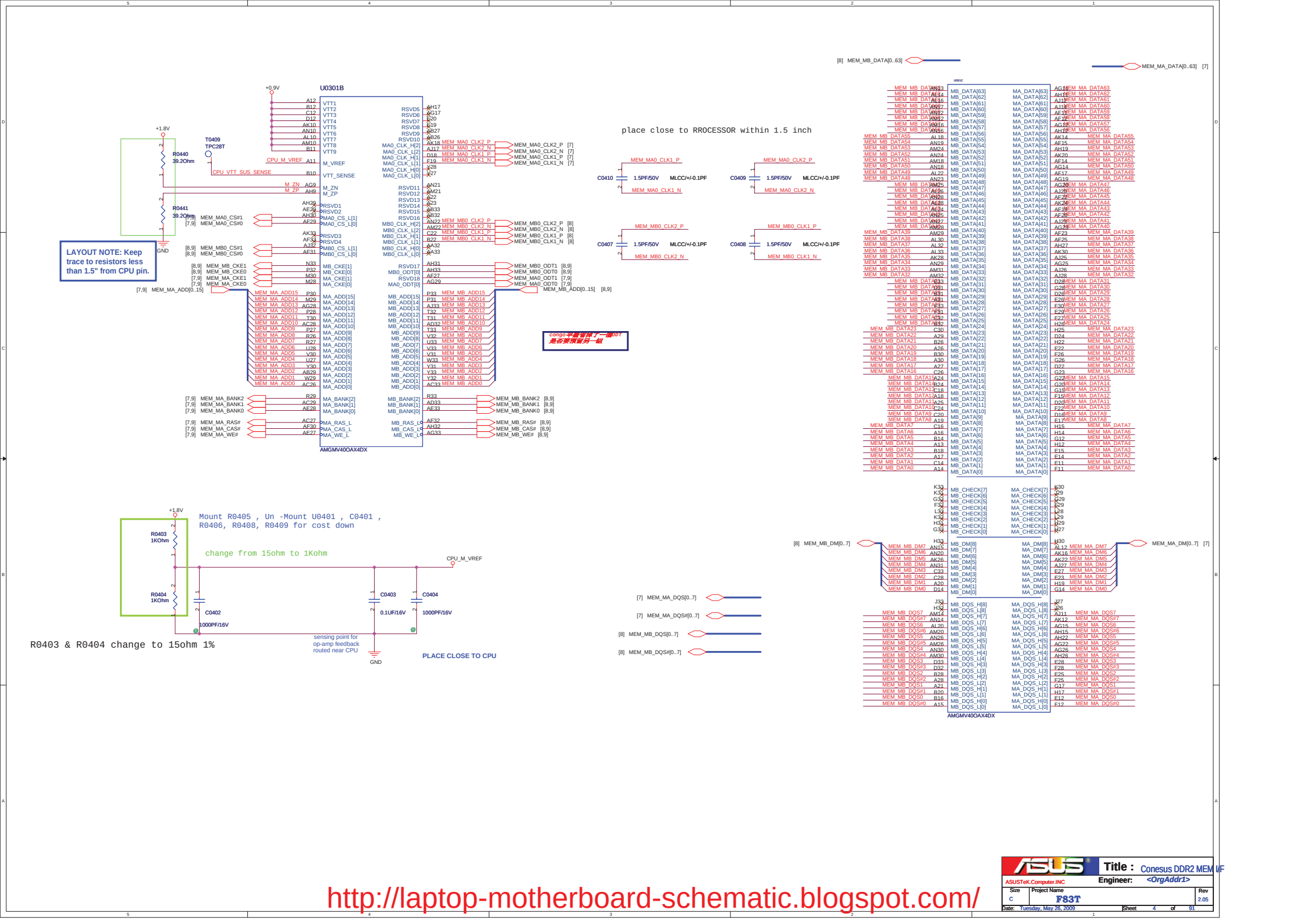
ASUSTeK.Computer.INC	Title : Power sequence		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F83T		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 2 of 91		

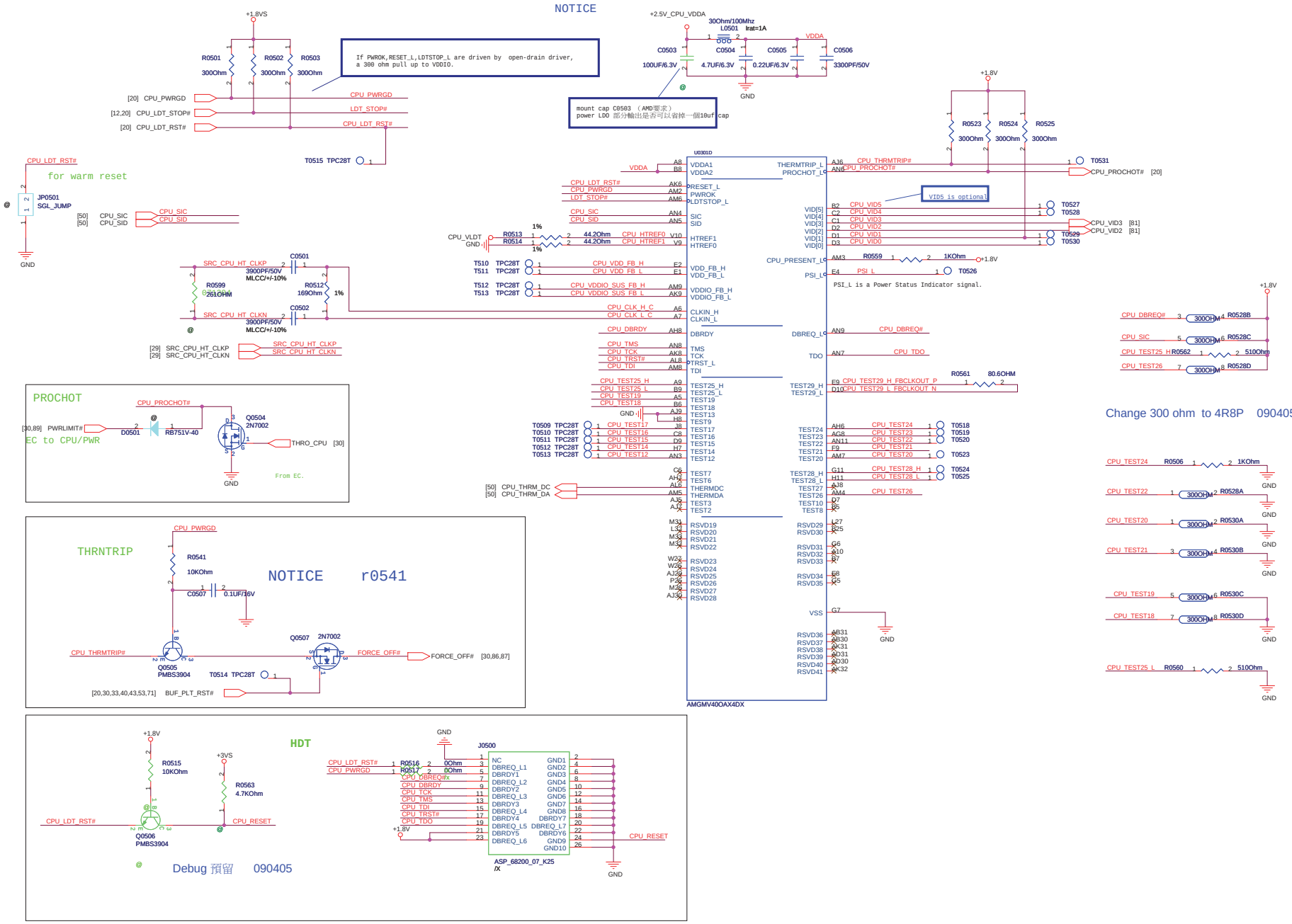


DESIGN NOTE:
VLDT must be routed as a pour or a trace at least 200 mils wide.
VLDT may be routed from the source to either ALx balls or Fx balls.
Choose whichever makes routing simpler.
These six capacitors must be placed very near the selected balls.
The "other" set of balls must be decoupled with a 4.7uF cap.

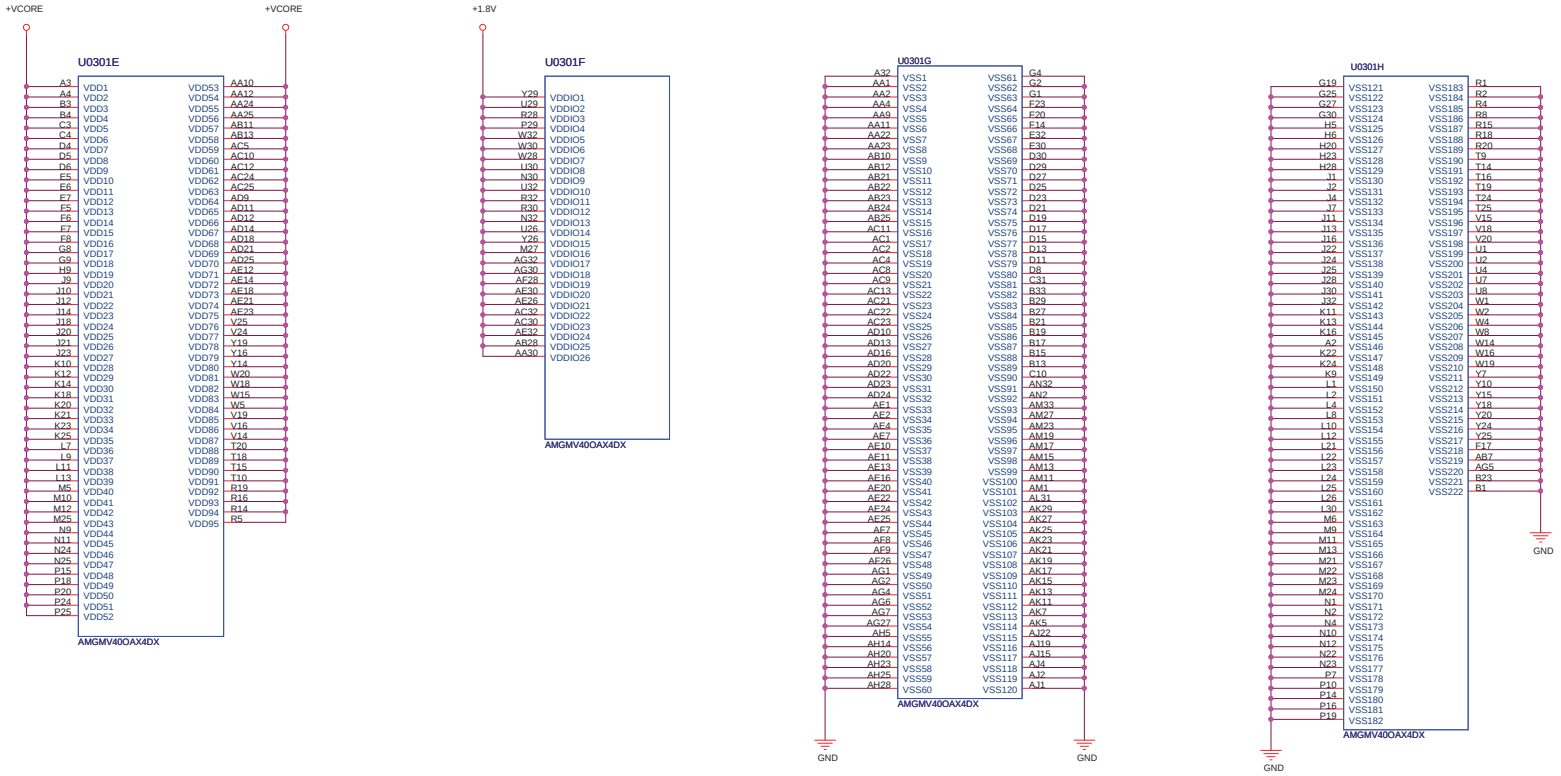


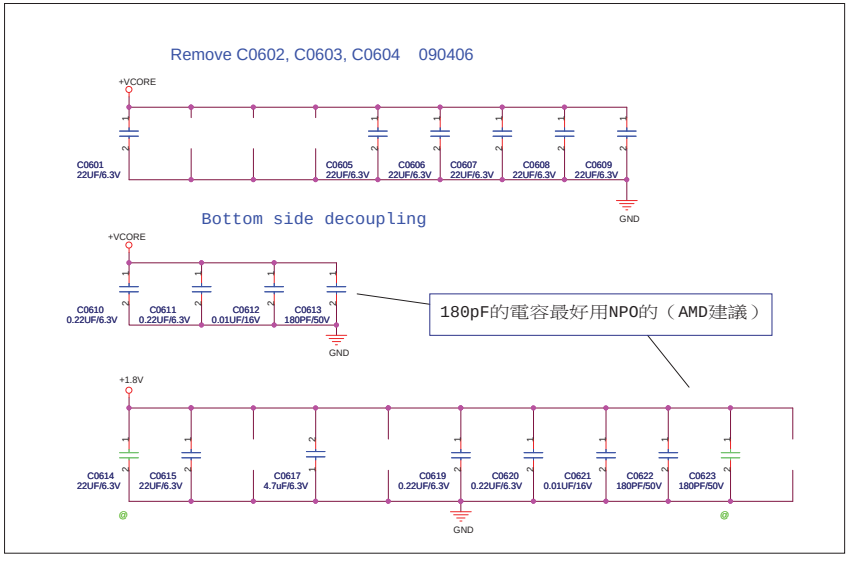
ASUSTeK.Computer.INC	Title : Conesus HT I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F83T	Rev: 2.05
Date: Friday, May 29, 2009	Sheet 3 of 91	

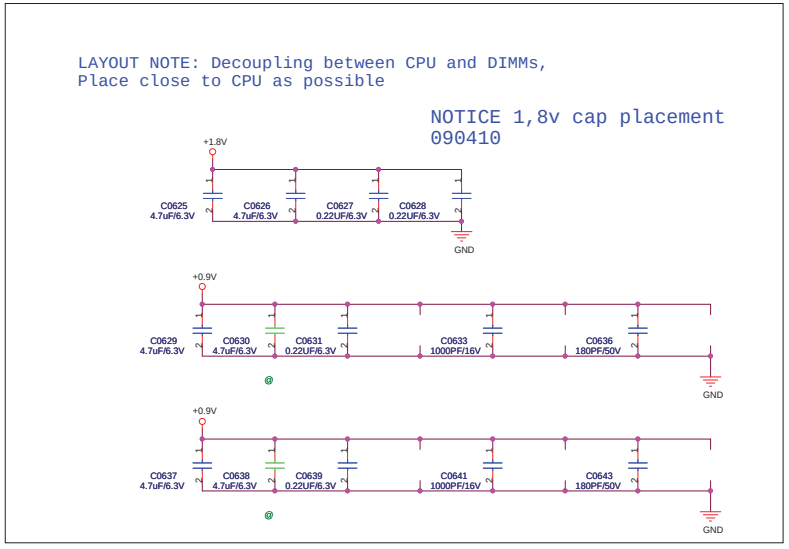

U0301B
AMGMV40OAX4DX
place close to RROCESSOR within 1.5 inch
LAYOUT NOTE: Keep trace to resistors less than 1.5" from CPU pin.
Mount R0405 , Un -Mount U0401 , C0401 , R0406, R0408, R0409 for cost down
change from 15ohm to 1Kohm
R0403 & R0404 change to 15ohm 1%
sensing point for op-amp feedback routed near CPU
PLACE CLOSE TO CPU
http://laptop-motherboard-schematic.blogspot.com/
Title : Conesus DDR2 MEM I/F
Engineer: <OrgAddr1>
ASUSTeK.Computer.INC
F83T
Rev 2.05
Tuesday, May 26, 2009
Sheet 4 of 91



ASUSTeK.Computer.INC	Title	Conesus CNT/DBG/THERM
	Engineer:	<OrgAddr1>
Size: C	Project Name: F83	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 5 of 91	







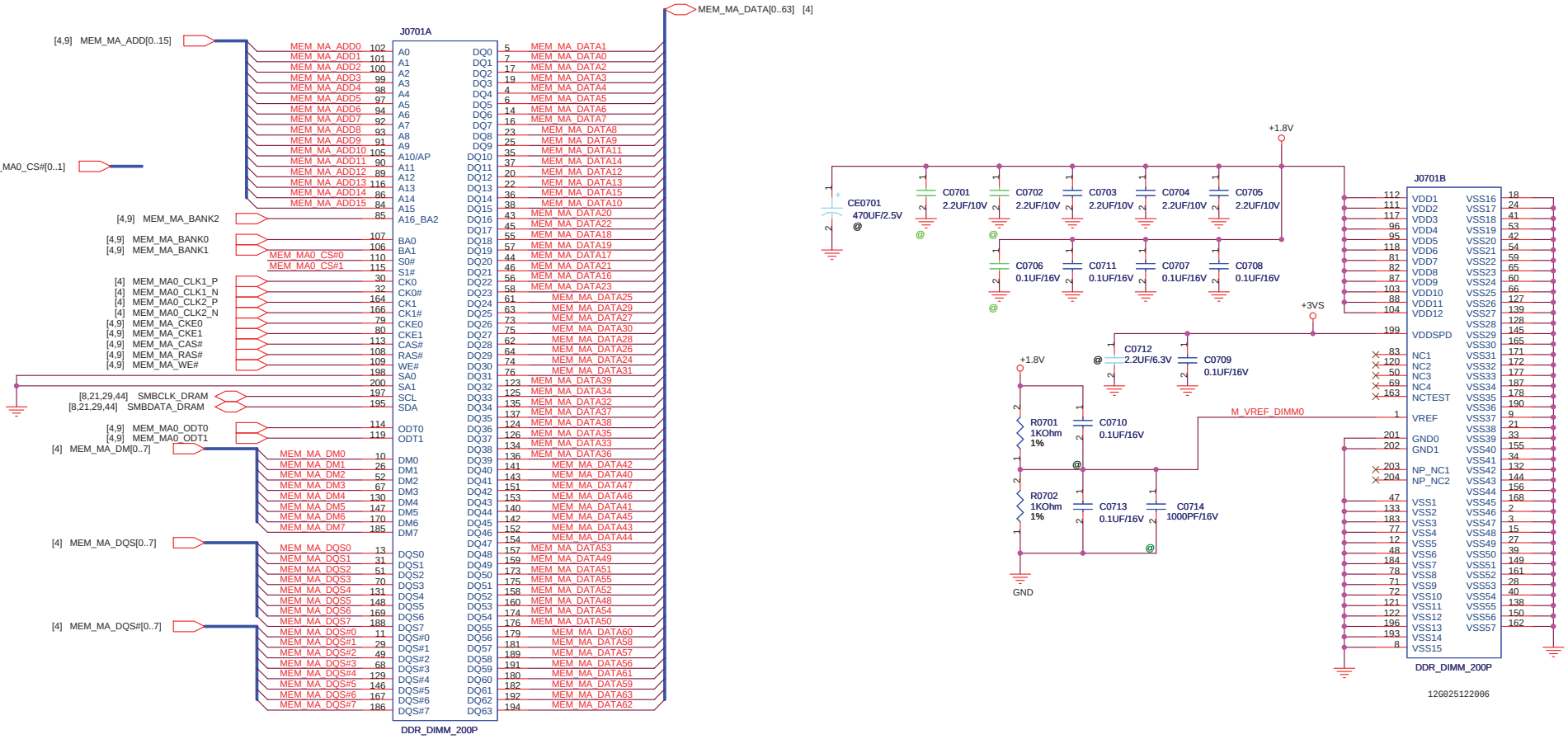
ASUSTeK.Computer.INC

Title : Conesus Power

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	F83	2.05

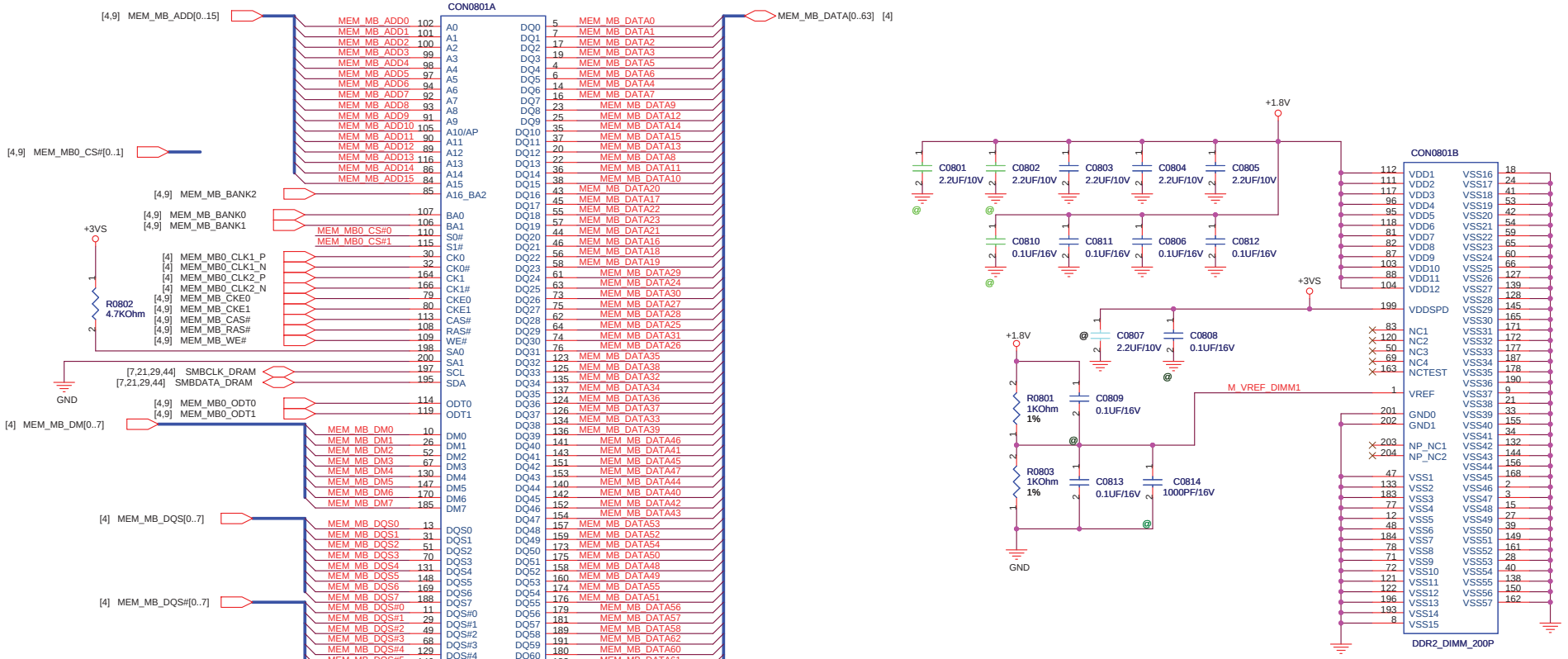
Date: Tuesday, May 26, 2009 Sheet 6 of 91



P/N:12G025122006

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM0	
	Engineer:	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 7 of 91	



PN:12G025C22003
REV.

ASUSTeK COMPUTER INC	Title : DDR2 SO-DIMM1		
	Engineer:		
Size: Custom	Project Name: F83T		Rev: 2.05
Date: Tuesday, May 26, 2009		Sheet 8 of 91	

change to 8R16P 090405

[4,7] MEM_MA_ADD[0..15]

071219
Del Bank2 to Bus

MEM_MA_ADD1 — 47OHM — RN0901C
MEM_MA_ADD3 — 47OHM — RN0901B
MEM_MA_ADD5 — 47OHM — RN0901A
MEM_MA_ADD8 — 47OHM — RN0903H

MEM_MA0_CS#1 — 47OHM — RN0901G
MEM_MA_CAS# — 47OHM — RN0901H
MEM_MA_WE# — 47OHM — RN0901E
MEM_MA_ADD9 — 47OHM — RN0903C
MEM_MA_ADD12 — 47OHM — RN0903D
MEM_MA_BANK2 — 47OHM — RN0903E
MEM_MA_CKE0 — 47OHM — RN0903B
MEM_MA_ADD7 — 47OHM — RN0901D
MEM_MA_ADD14 — 47OHM — RN0903G
MEM_MA_ADD15 — 47OHM — RN0903F
MEM_MA_CKE1 — 47OHM — RN0903A

MEM_MA_RAS# — 47OHM — RN0901F
MEM_MA_BANK1 — 47OHM — RN0905D
MEM_MA_ADD4 — 47OHM — RN0905H

MEM_MA0_ODT0 — 47OHM — RN0905C
MEM_MA_ADD13 — 47OHM — RN0905A
MEM_MA0_CS#0 — 47OHM — RN0905B

MEM_MA_ADD2 — 47OHM — RN0905F
MEM_MA_ADD6 — 47OHM — RN0905G

MEM_MA_ADD0 — 47OHM — RN0905E
MEM_MA_ADD11 — 47Ohm — RN0909C

MEM_MA0_ODT1 — 47Ohm — RN0909D

MEM_MA_BANK0 — 47Ohm — RN0909A
MEM_MA_ADD10 — 47Ohm — RN0909B

+0.9V
C0901 0.1UF/16V +1.8V
C0902 0.1UF/16V +1.8V
C0903 0.1UF/16V +1.8V
C0912 0.1UF/16V +1.8V
C0913 0.1UF/16V +1.8V
C0914 0.1UF/16V +1.8V
C0915 0.1UF/16V +1.8V
C0916 0.1UF/16V +1.8V

是否用排容？
090330

Remove1.8V C0910,C0911 0.1uF 090405

+0.9V
0.1UF/16V C0904
0.1UF/16V C0905
0.1UF/16V C0906
0.1UF/16V C0907
0.1UF/16V C0908
0.1UF/16V C0909
GND

071207

[4,7] MEM_MA_BANK2 — MEM_MA_BANK2
[4,7] MEM_MA_BANK1 — MEM_MA_BANK1
[4,7] MEM_MA_BANK0 — MEM_MA_BANK0

[4,7] MEM_MA0_ODT0 — MEM_MA0_ODT0
[4,7] MEM_MA0_ODT1 — MEM_MA0_ODT1

[4,7] MEM_MA_CKE0 — MEM_MA_CKE0
[4,7] MEM_MA_CKE1 — MEM_MA_CKE1

[4,7] MEM_MA_RAS# — MEM_MA_RAS#
[4,7] MEM_MA_CAS# — MEM_MA_CAS#
[4,7] MEM_MA_WE# — MEM_MA_WE#

[4,7] MEM_MA0_CS#0 — MEM_MA0_CS#0
[4,7] MEM_MA0_CS#1 — MEM_MA0_CS#1

add MA0_ODT1音MB0_ODT1
090417

change to 8R16P 090405

[4,8] MEM_MB_ADD[0..15]

MEM_MB_ADD14 — 47OHM — RN0912F
MEM_MB_ADD7 — 47OHM — RN0912A
MEM_MB_ADD11 — 47OHM — RN0912E
MEM_MB_ADD12 — 47OHM — RN0912B
MEM_MB_ADD10 — 47OHM — RN0910E
MEM_MB_ADD0 — 47OHM — RN0910G
MEM_MB0_ODT0 — 47OHM — RN0910A
MEM_MB_ADD13 — 47OHM — RN0910B
MEM_MB_RAS# — 47OHM — RN0910D
MEM_MB0_CS#0 — 47OHM — RN0910C
MEM_MB_ADD1 — 47OHM — RN0912E
MEM_MB_ADD2 — 47OHM — RN0910H
MEM_MB_ADD15 — 47OHM — RN0912G
MEM_MB_CKE1 — 47OHM — RN0912H
MEM_MB_BANK2 — 47OHM — RN0912C
MEM_MB_CKE0 — 47OHM — RN0912D

MEM_MB0_CS#1 — 47OHM — RN0914H
MEM_MB_CAS# — 47OHM — RN0914G

MEM_MB_ADD8 — 47OHM — RN0914A
MEM_MB_ADD3 — 47OHM — RN0914D
MEM_MB_ADD6 — 47OHM — RN0914C

MEM_MB_WE# — 47OHM — RN0914F
MEM_MB_BANK0 — 47OHM — RN0910F

MEM_MB_ADD4 — 47OHM — RN0914B
MEM_MB_ADD9 — 47Ohm — RN0916D

MEM_MB0_ODT1 — 47Ohm — RN0916B

MEM_MB_ADD5 — 47Ohm — RN0916C
MEM_MB_BANK1 — 47Ohm — RN0916A

+0.9V
C0917 0.1UF/16V +1.8V
C0918 0.1UF/16V +1.8V
C0919 0.1UF/16V +1.8V
C0927 0.1UF/16V +1.8V
C0929 0.1UF/16V +1.8V
C0930 0.1UF/16V +1.8V
C0931 0.1UF/16V +1.8V
C0932 0.1UF/16V +1.8V

Remove1.8V C0926,C0928 0.1uF 090405

+0.9V
0.1UF/16V C0920
0.1UF/16V C0921
0.1UF/16V C0922
0.1UF/16V C0923
0.1UF/16V C0924
0.1UF/16V C0925
GND

071211

[4,8] MEM_MB_BANK2 — MEM_MB_BANK2
[4,8] MEM_MB_BANK1 — MEM_MB_BANK1
[4,8] MEM_MB_BANK0 — MEM_MB_BANK0

[4,8] MEM_MB0_ODT0 — MEM_MB0_ODT0
[4,8] MEM_MB0_ODT1 — MEM_MB0_ODT1

[4,8] MEM_MB_CKE0 — MEM_MB_CKE0
[4,8] MEM_MB_CKE1 — MEM_MB_CKE1

[4,8] MEM_MB_RAS# — MEM_MB_RAS#
[4,8] MEM_MB_CAS# — MEM_MB_CAS#
[4,8] MEM_MB_WE# — MEM_MB_WE#

[4,8] MEM_MB0_CS#0 — MEM_MB0_CS#0
[4,8] MEM_MB0_CS#1 — MEM_MB0_CS#1

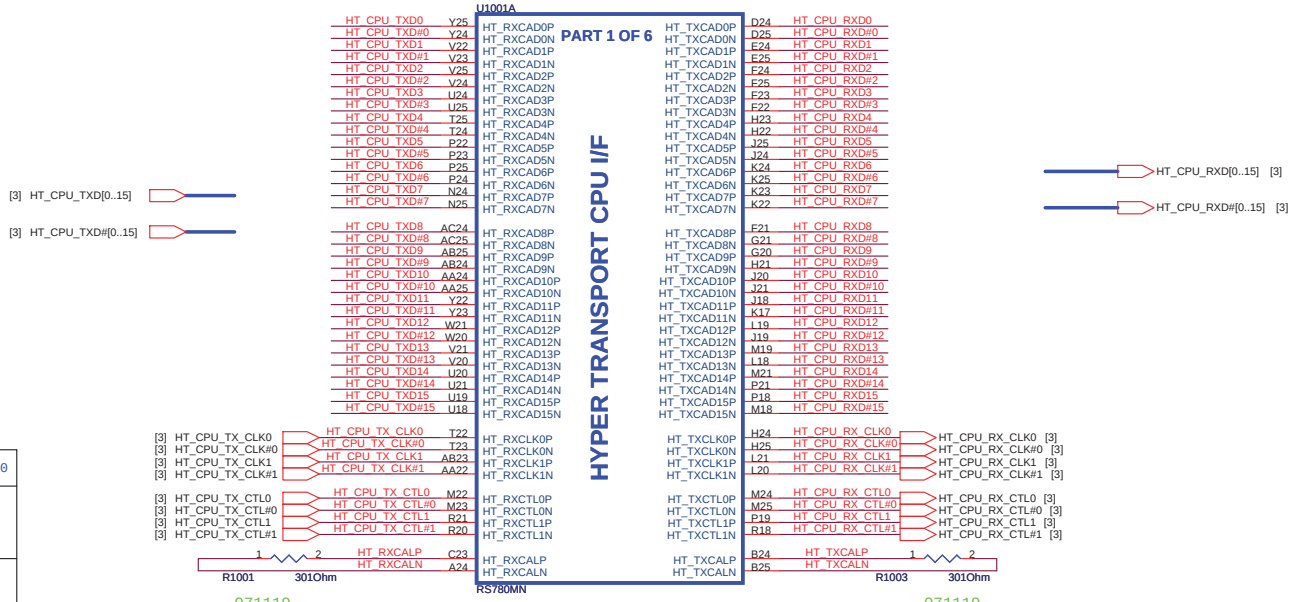
add MA0_ODT1音MB0_ODT1
090417

+1.8V
0.1UF/16V C0933
0.1UF/16V C0934
0.1UF/16V C0935
0.1UF/16V C0936
0.1UF/16V C0937
0.1UF/16V C0938
GND

PLACE CLOSE TO SOCKET(PER EMI/EMC)

ASUSTeK COMPUTER INC
Title : DDR2_TERMINATIONS
Engineer:
Size: Custom
Project Name: J5JZ
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 9 of 91

R1.11 080319
Change the NB Part number to RS780 (A13)



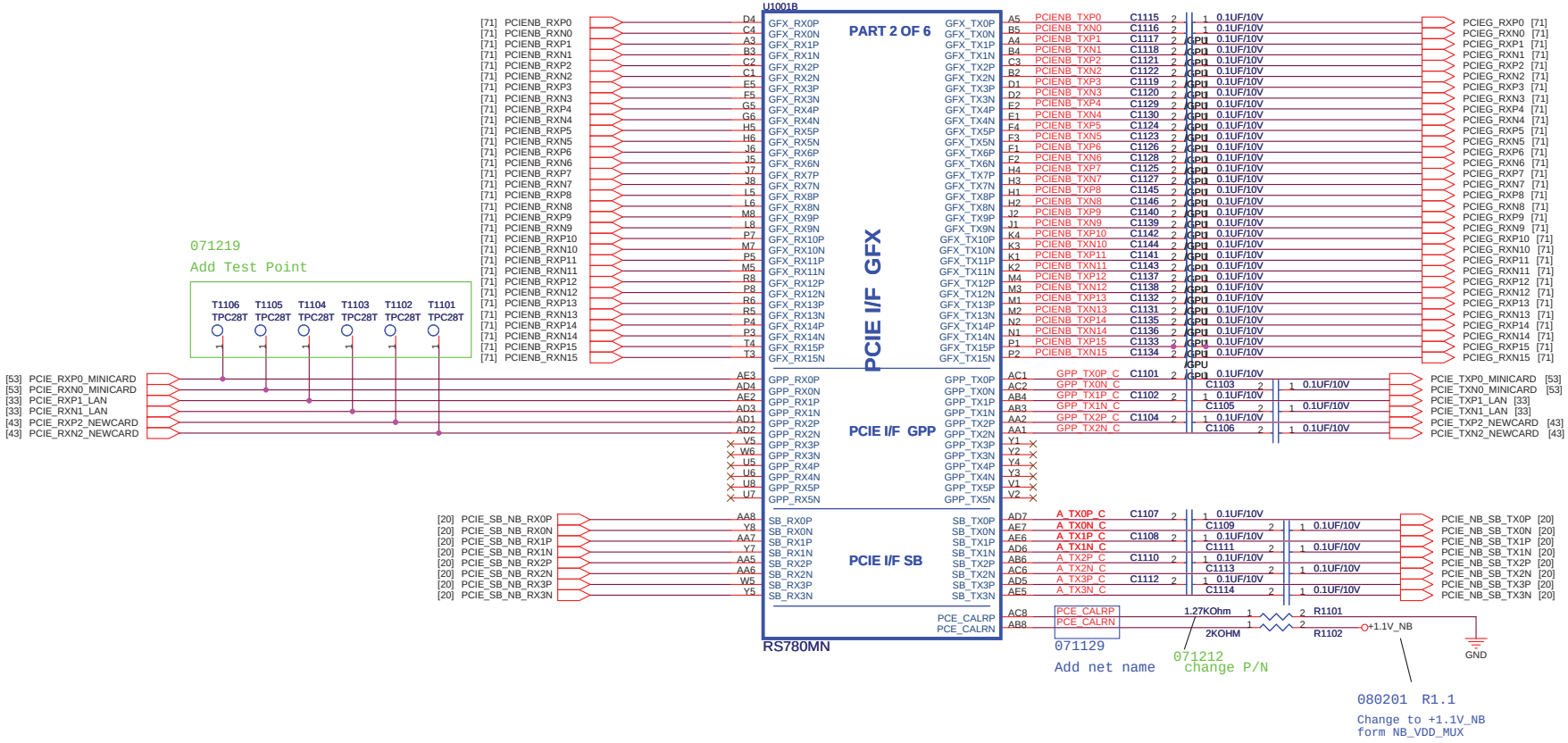
Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

071119
change R1001 value

071119
change R1003 value

ASUSTeK.Computer.INC	Title : RS780M-HT LINK I/F	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 10 of 91	

R1.11 080319
Change the NB Part number to RS780 (A13)



ASUSTeK.Computer.INC	Title : RS780M-PCIE LINK I/F		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F5Z		Rev: 2.05
Date: Friday, May 29, 2009	Sheet 11 of 91		

notice L1201 L1204 change SL?
090411

U1001C
PART 3 OF 6
RS780MN

CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.

090407
071219
For Layout impdance setting

R1.11
080310

080201 R1.1
Change to +1.1V_NB
form NB_VDD_MUX

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

Notice RN1215 remove ?
090411

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

071115
090316
change backlight control by M92
071207
remove D1201 circuit
090410
071116

R1.11
080319
Change the NB Part number to RS780 (A13)

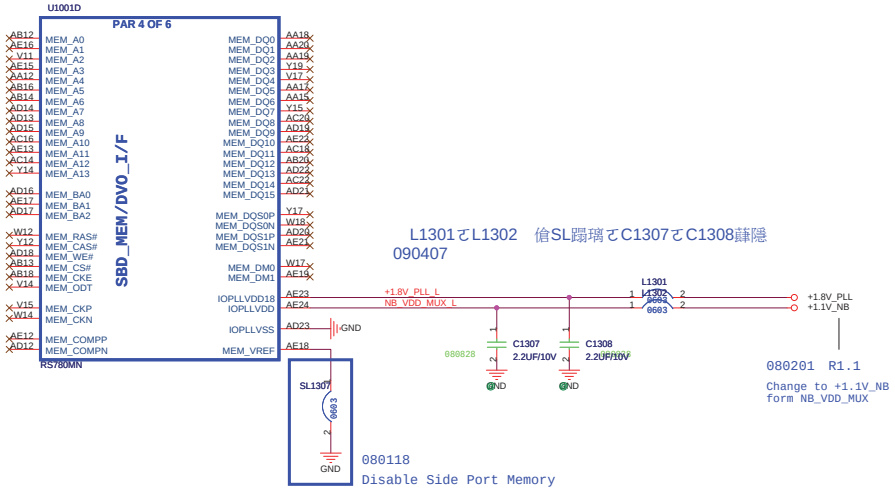
080325
R2.0 Remove Q1201A and R1219

071218
for measurement near U1001
071204
DEL serial R
?? for external graphic
have via for measurement

ASUSTeK.COMPUTER.INC
Title : RS780M-SYS I/F
Engineer: <OrgAddr1>
Size: C
Project Name: F5Z
Rev: 2.05
Date: Tuesday, May 26, 2009
Sheet 12 of 91

R1.11 080319

Change the NB Part number to RS780 (A13)



L1301ぞL1302　傖SL蹋璃ぞC1307ぞC1308蘚隠

090407

080201 R1.1

Change to +1.1V_NB form NB_VDD_MUX

080118

Disable Side Port Memory

R1.1

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

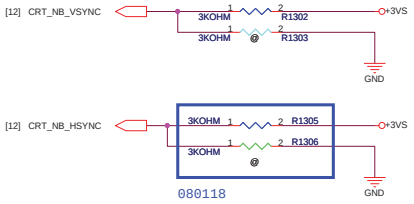
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```

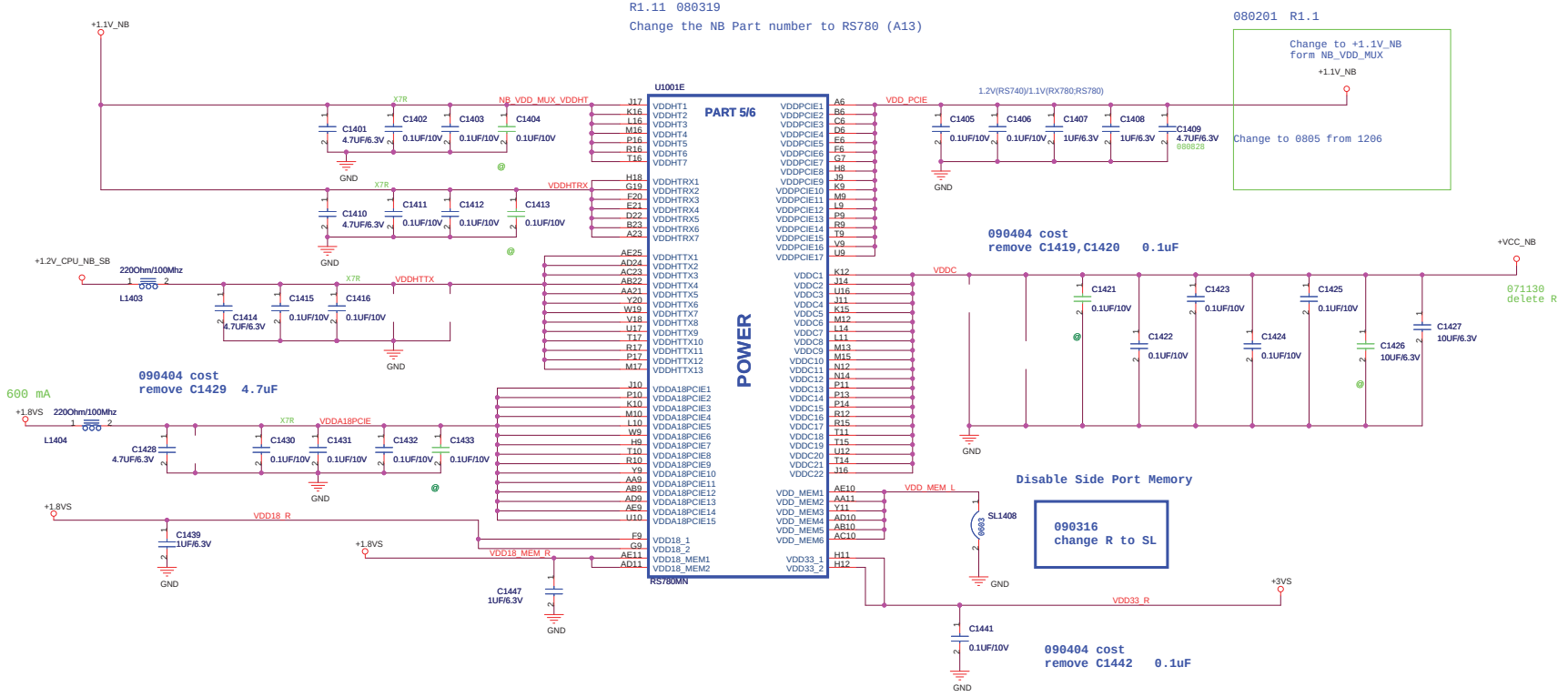


080118

Disable Side Port Memory

R1.1

ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 13 of 91	



ASUSTeK.COMPUTER.INC	Title : RS780M-POWER	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 14 of 91	

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 15 of 91	

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 16 of 91

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 17 of 91	

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 18 of 91

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 19 of 91

R2.0 080327
Add test point for factory
ICT test

R1.11 080319
Change the SB Part number to SB700 (A12)

071120
add net name

071204
AMD review

080130 R1.1
Change TPM CLK

SB700
Part 1 of 5

U2001A

PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC

071212
change P/N

090403

071121

Correct to R1.1

071218
for measurement
near U2001
del R2007,R2011

080212
R1.1
Del T2017~T2033 for
GND Via improvement

080212
R1.1
Del T2052~T2074 for
GND Via improvement

080218 R1.1
Add Test Point

Reserved Via

080218 R1.1
Add Test Point

internal Pull Up 15K

標注
internal Pull Up 8.2K

Add net SB_OSC
090326

080130 R1.1 Change TPM CLK

071204
AMD review

STRAP 071119

EMI
090414

R2.0 080327
Add test point for factory
ICT test

change C2015,C2016 to 22pF 090407

做BOM時要更換成SB710的料號:02G050003001
090406

R2.02 080519
Un-Mount D2001 and Mount R2035.
080526
Change R2035 P/N form 10G212000004030 to 10G212000004070 for ECN requirement

Change the P/N of BAT2001 from
12G201100203 to 12G201100208

change ctystal (SB710) 07G010413277
090331

ASUSTeK.Computer.INC	Title : SB700_CPU/PCIE/LPC/CLK	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 20 of 91	

R1.11 080319
Change the SB Part number to SB700 (A12)

071129
Add net name

USB [3:0] ->USB PORT
USB 4 -> NEW CARD
USB 6 -> CAMERA
USB 10 -> CARDREADER
USB 12 -> BT Module

U2001D
SB700
Part 4 of 5

071114
071113
071119
071204
071207
RS780 POWERGOOD
is 1.8VS rail
+1.8VS
R2137 300OHm
(I / PU)
T2101 TPC28T
T2105 TPC28T
T2107 TPC28T
T2106 TPC28T
T2108 TPC28T
T2117 TPC28T
T2121 TPC28T
SYS_REST#
SB_THRMTRIP#
NB_PWRGD_R
PM_RSMRST#_EC
[12] NB_PWRGD
[30] EXT_SMI#
[30] EXT_SCI#
[30] PM_SUSB#
[30] PM_SUSC#
[30] PM_PWRBTN#
[30] PM_PWROK_EC
[12] SUS_STAT#
[30] A20GATE
[30] RC_IN#
[43,44] CPPE_DET#
[33,43,53] PCIE_WAKE#
[30] PM_RSMRST#_EC

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USBCLK_48_SB
USBCLK_48 [29]
R2104 11.8KOhm r0603_h24
GND

USB MISC

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_PP13 [61]
USB_PN13 [61]
USB_PP12 [61]
USB_PN12 [61]
Fingerprint
Bluetooth

USB 1.1

USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_PP10 [40]
USB_PN10 [40]
AU6433

USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_PP6 [45]
USB_PN6 [45]
CCD

USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_PP4 [43]
USB_PN4 [43]
NewCard

USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_PP2 [52]
USB_PN2 [52]
USB_HSD1P
USB_HSD1N
USB_PP1 [52]
USB_PN1 [52]
USB_HSD0P
USB_HSD0N
USB_PP0 [52]
USB_PN0 [52]
USB CONN

USB 2.0

071203
AMD review
SUS_STAT#
R2110 4.7KOhm
GND

071119
S0 power
+3VS
SUS_STAT#
R2109 4.7KOhm
SMBCLK_DRAM
SMBDATA_DRAM
RN2112C 2.2KOHM
RN2112D 2.2KOHM

090404 cost

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT1/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3 /GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3 /GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SMARTVOLT2/SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

GPIO

T2118 TPC28T
T2102 TPC28T
T2109 TPC28T
T2103 TPC28T
T2110 TPC28T
T2123 TPC28T
T2113 TPC28T
T2111 TPC28T
T2104 TPC28T
T2112 TPC28T
SB_SPKR
SB_SPKR_R
GPIO10
GPIO6
PCB_ID1
GPIO0
GPIO39
GPIO40
GPIO8
GPIO66
PCB_ID2
DDR3_RST# Via
[7,8,29,44] SMBCLK_DRAM
[7,8,29,44] SMBDATA_DRAM
[7,8,29,44] SMBDATA_NEWCARD
[7,8,29,44] SMBCLK_NEWCARD

R2.0 080401
Add R2108 and R2113 for SMBCLK_NEWCARD and SMBDATA_NEWCARD.

080118 Reserve Via

071114
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
[43] USB_OC4_NEWCARD#
T2114 TPC28T
T2116 TPC28T
[52] USB_OC1#
[52] USB_OC0#

USB OC

080212 R1.1
Del T2115 and T2116 for GND Via
improvement (GPIO44 and 46)

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
ACZ_BCLK
ACZ_SDOUT
[36] ACZ_SDIN0_AUD
ACZ_SYNC
ACZ_RST#
GPM8# VIA
T2115 TPC28T
080218 R1.1
Add Test Point

HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
T2119 TPC28T
T2120 TPC28T
SPI_CS2#

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
SMBCLK_SYS [53]
SMBDATA_SYS [53]
T2122 T2124
071204 AMD review
FOR MINICARD/NEWCARD
SB_GP16 [24]
SB_GP17 [24]
for strap
TPC28T
TPC28T

IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

INTEGRATED uC

INTEGRATED uC

071204 AMD review
+3VSUS
SMBCLK_SYS
SMBDATA_SYS
RN2112A 2.2KOHM
RN2112B 2.2KOHM
TEST2 R2120 2.2kOHM
TEST1 R2121 2.2kOHM
TEST0 R2132 2.2kOHM
071204 AMD review

internal P/U 8.2k
[22] PCB_ID0
PCB_ID2
PCB_ID1
PCB_ID0
R2117 4.7KOhm
R2118 4.7KOhm
R2119 4.7KOhm

R2.01 080411
Change P/N to
10G212472004010

080215 R1.1
change 4.7K P/N from
10G212472004040 to
10G212472004010

R2.0 080402
Mount R2117 and un-monent
R2118 for PCB ID

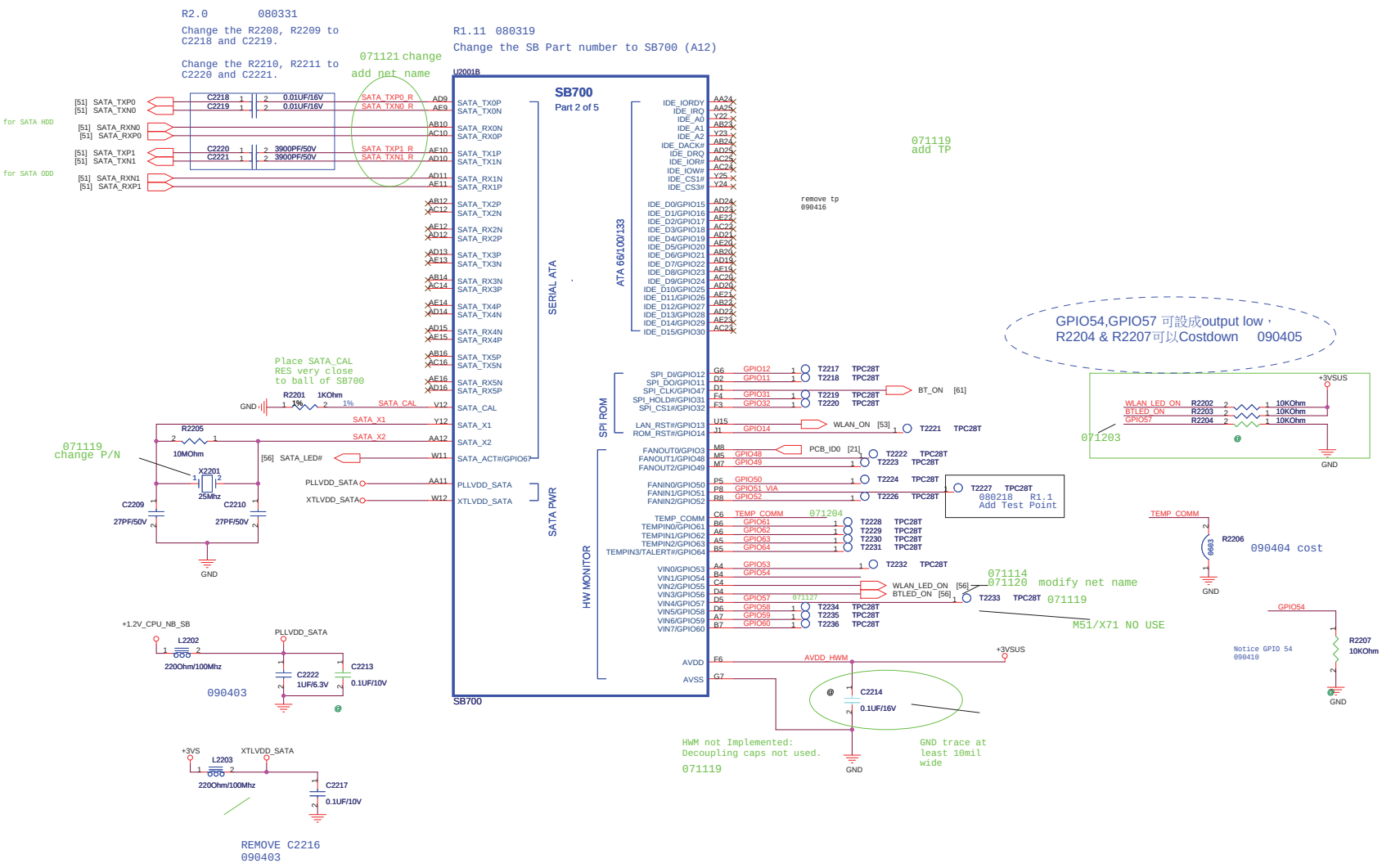
071120
res. value 10k -> 4.7k to
get LOW level < Vih(1.8V)

071204
AMD review
ACZ_SDIN0_AUD
R2134 10KOhm

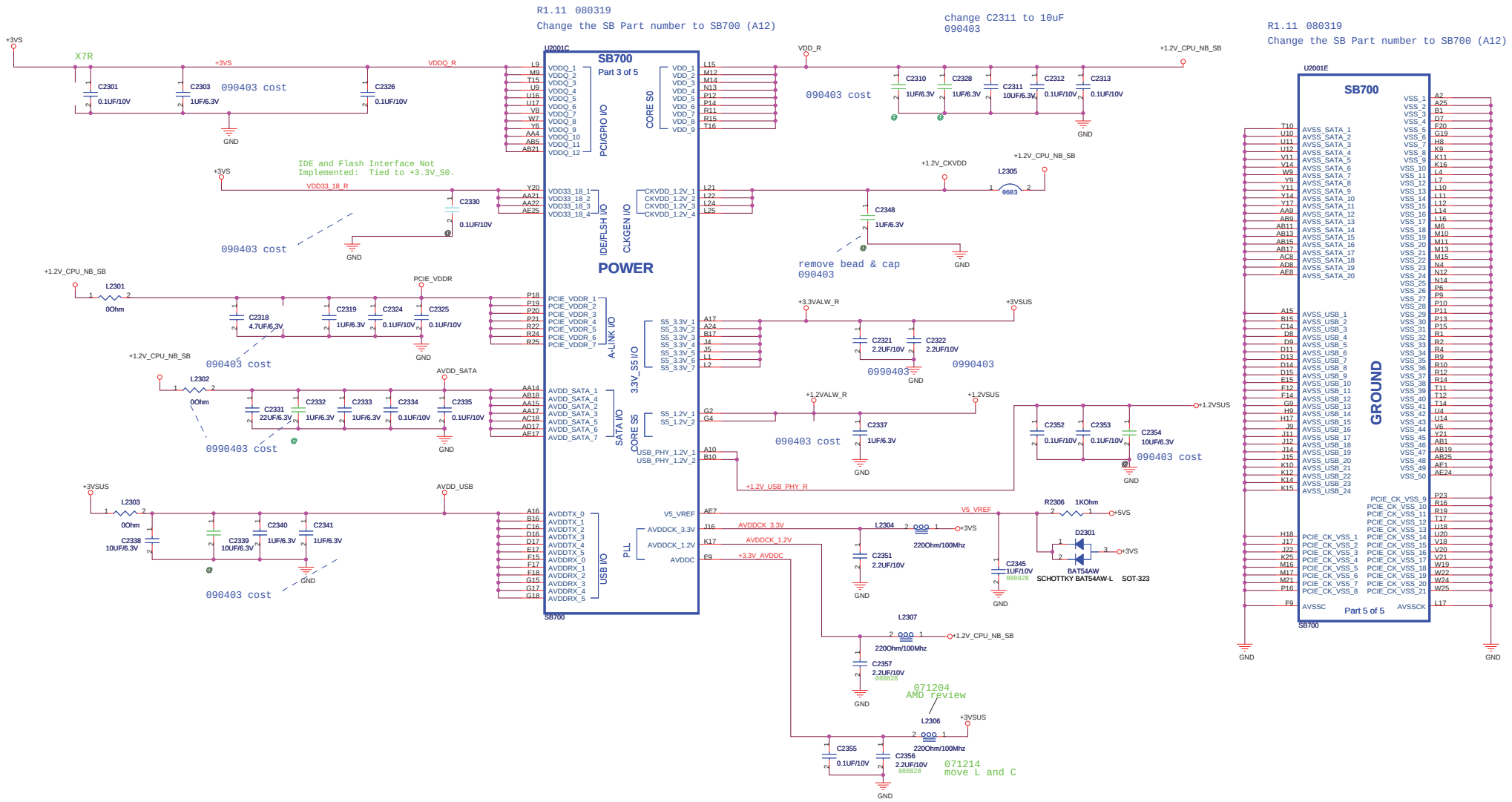
PUT AT SB700 SIDE
Change 33ohm to 4R8P 090405
for strap
[24] ACZ_RST#
R2123A 33OHM
ACZ_RST# AUD
ACZ_RST#_AUD [36,37]
SB700A11 EC enable Strap Workaround
EMI 090415
C2148 22PF/50V /EMI
ACZ_BCLK
R2123D 33OHM
ACZ_BCLK_AUD
ACZ_BCLK_AUD [36]
R2133 10KOhm
AMD review
ACZ_SYNC
R2123B 33OHM
ACZ_SYNC_AUD
ACZ_SYNC_AUD [36]
ACZ_SDOUT
R2123C 33OHM
ACZ_SDOUT_AUD
ACZ_SDOUT_AUD [36]

need to modify topology??

ASUSTeK.Computer.INC
Title : SB700_GPIO/USB/HD/ACPI
Engineer: <OrgAddr1>
Size C
Project Name F5Z
Rev 2.05
Date: Tuesday, May 26, 2009
Sheet 21 of 91



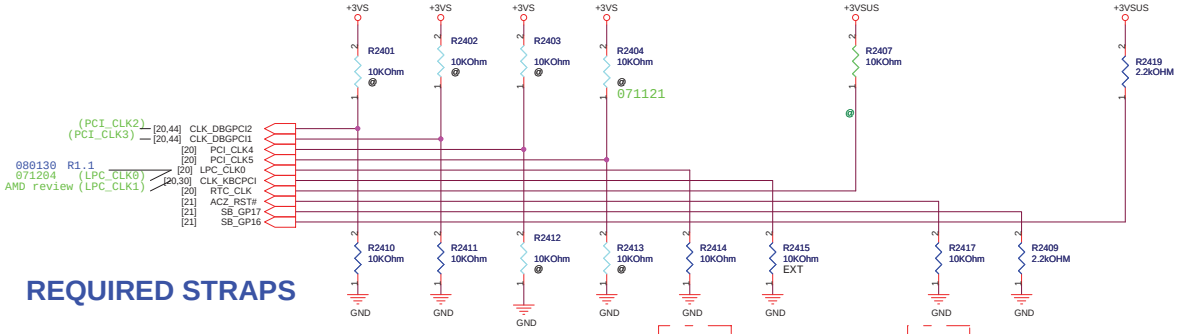
ASUSTeK.COMPUTER.INC	Title : SB700_PATA/SATA	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 22 of 91	



ASUSTeK.Computer.INC	Title : SB700_POWER	
	Engineer: <OrgAddr1>	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 23 of 91	

Remove R2405, R2406,R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

For SB700 A12 and later version

080204 R1.1
Change the Text Comment

Remove EEPROM 090405

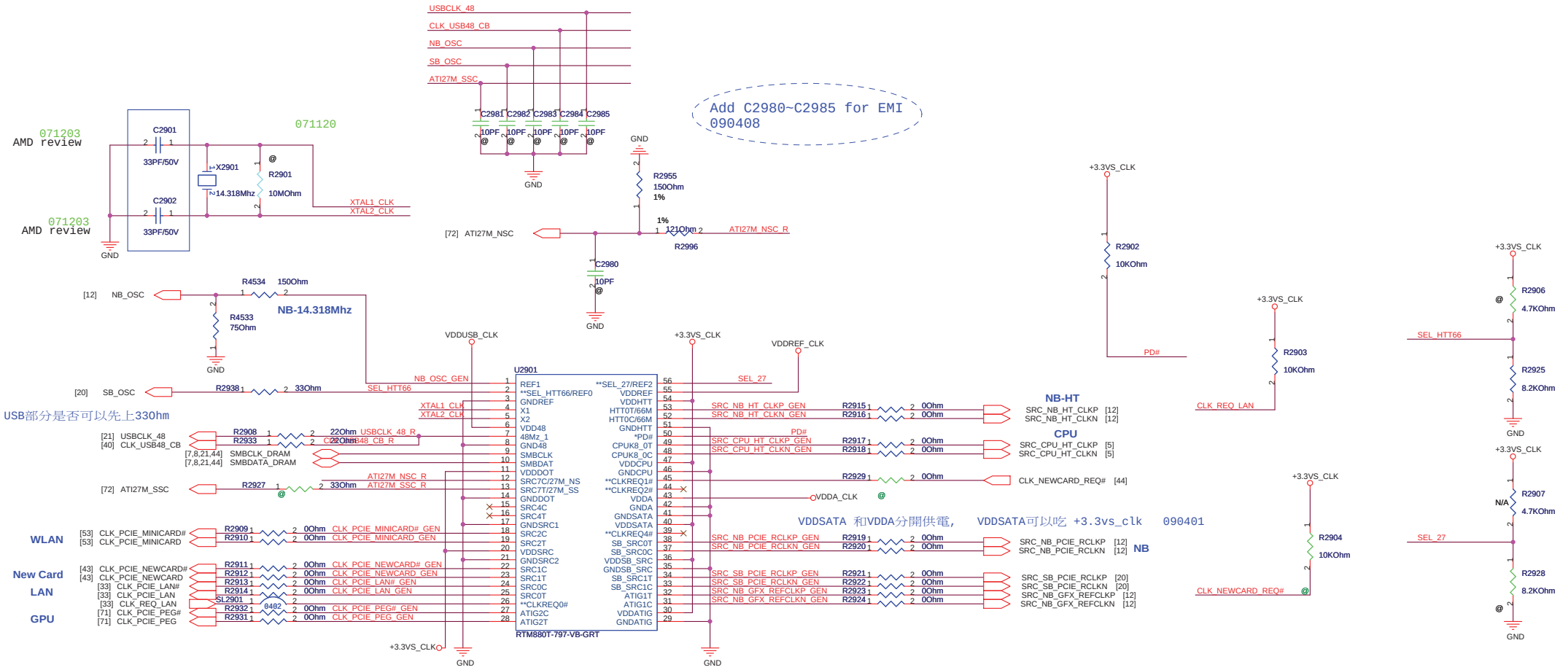
ASUSTeK.Computer.INC	Title : SB700_STRAP
	Engineer: <OrgAddr1>
Size: C	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 24 of 91

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 25 of 91	

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 26 of 91

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 27 of 91

ASUSTeK COMPUTER INC. NB1	Title :
	Engineer: <OrgAddr1>
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 28 of 91



SEL_27	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

ASUSTeK COMPUTER INC

Title : RTM880T-797-VB-GRT

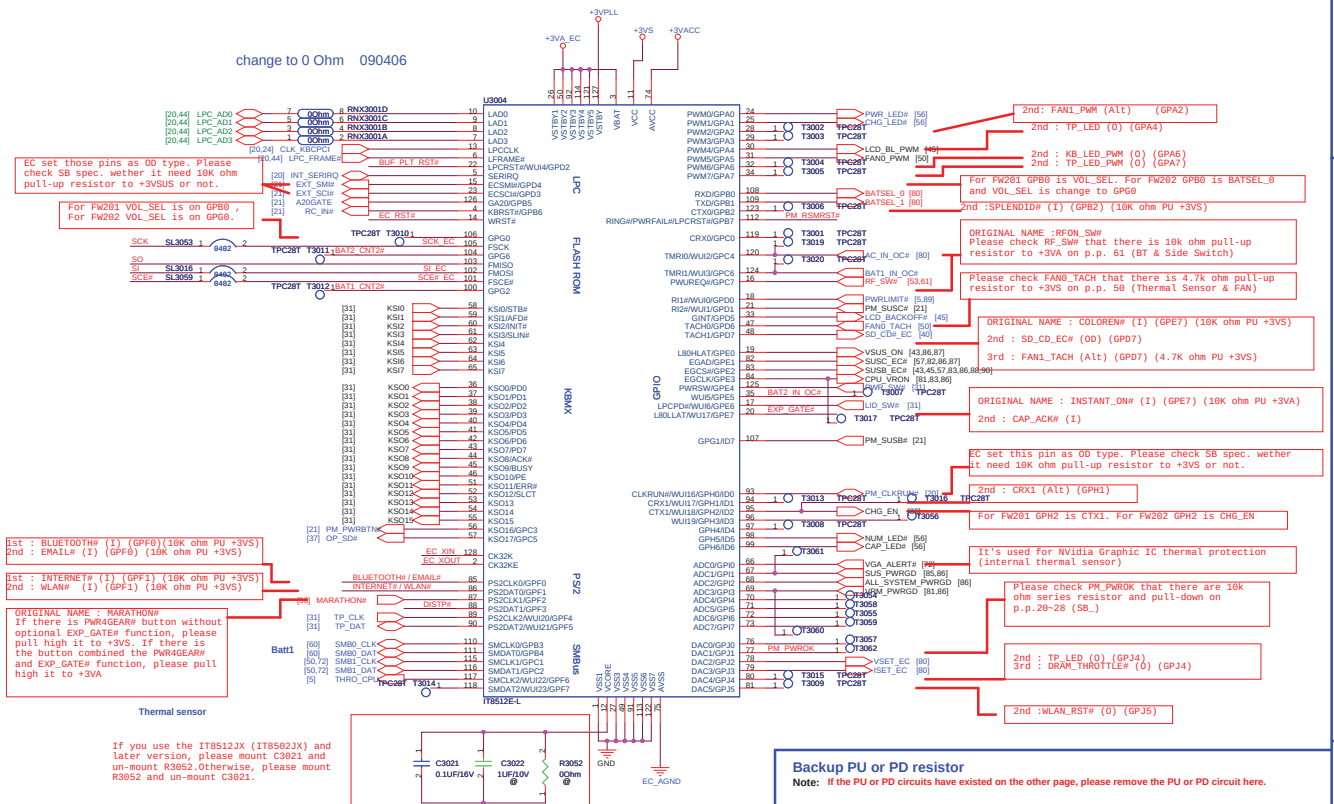
Engineer: xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.05

Date: Tuesday, May 26, 2009 Sheet 29 of 91

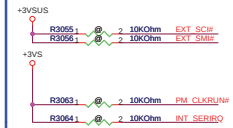
Notice EC FW 202
090410

change to 0 Ohm 090406



Backup PU or PD resistor

Note: If the PU or PD circuits have existed on the other page, please remove the PU or PD circuit here.

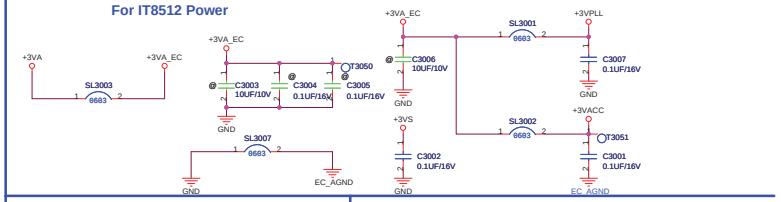


Fix for "Auto Power on" and "Data time error" Issue in Intel Platform

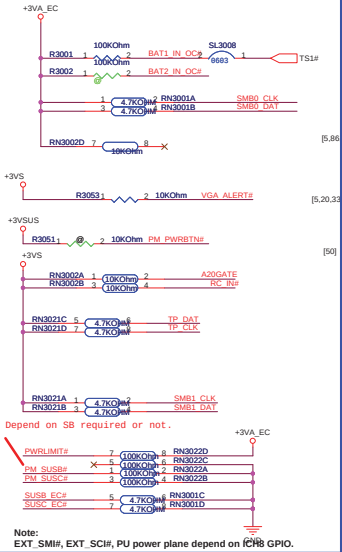
Note: If the schematic below has existed on pp.20~28 (SB_), please remove the circuit here.

To SB

For IT8512 Power



For PU / PD

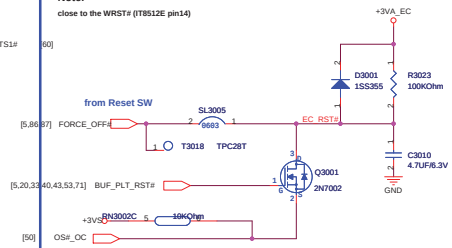


Depend on SB required or not.

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

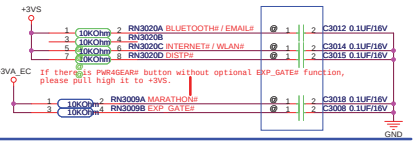
Note:
close to the WRST# (IT8512E pin14)



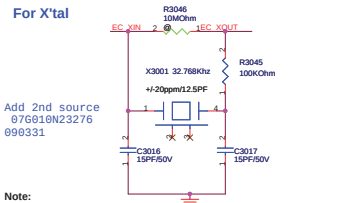
For Instant Key

Note: Close to EC

Please check there are de-bounce cap near the switch, then un-mount the cap here.



For X'tal



Add 2nd source
07G010N23276
090331

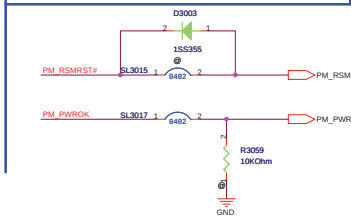
Note:
Cload place close to EC
Cload can be fine tune , and EC need X'tal to within typical +/- 100 ppm

For EC Hardware Strap

I/O Base Address
Note: It can be programmable by EC fireware

Share Memory
Note: It can be programmable by EC fireware.

PP Enable
Note: Default Int. Pull-Low



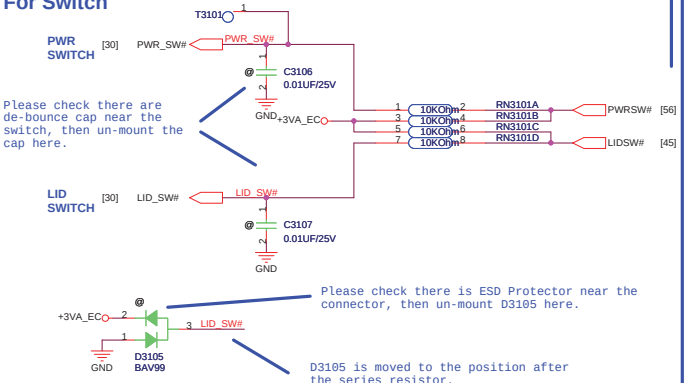
ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512 (1/2)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: F5Z		Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 30 of 91		

For Battery

Note: If there is the same circuit on pp.60 (DC & BAT IN), please delete the circuit here

Remove D3101 part circuit
090409

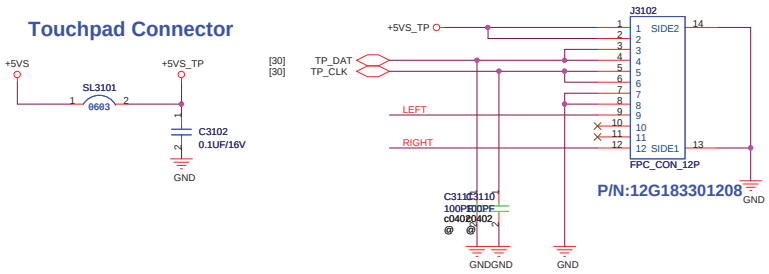
For Switch

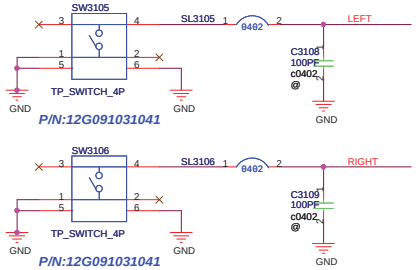


For Thermal Control Method

Note: Please follow the Thermal-Trip circuit on pp.3~6 (CPU_)

Touchpad Connector

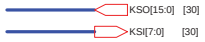




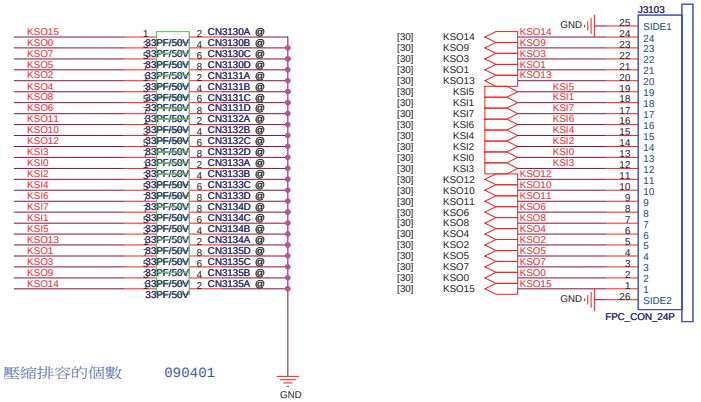
Notice switch P/N
090410

Keyboard Connector

Schematic below is noly the example in the previos project. It will be different between the different connector used in the Project.



Please follow the ASUS Keyboard Matrix Spec
Please Design based on your project.



壓縮排容的個數 090401

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8512 (2/2)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 31 of 91	

Remove all RST SCH and Change SW to other page

<Variant Name>

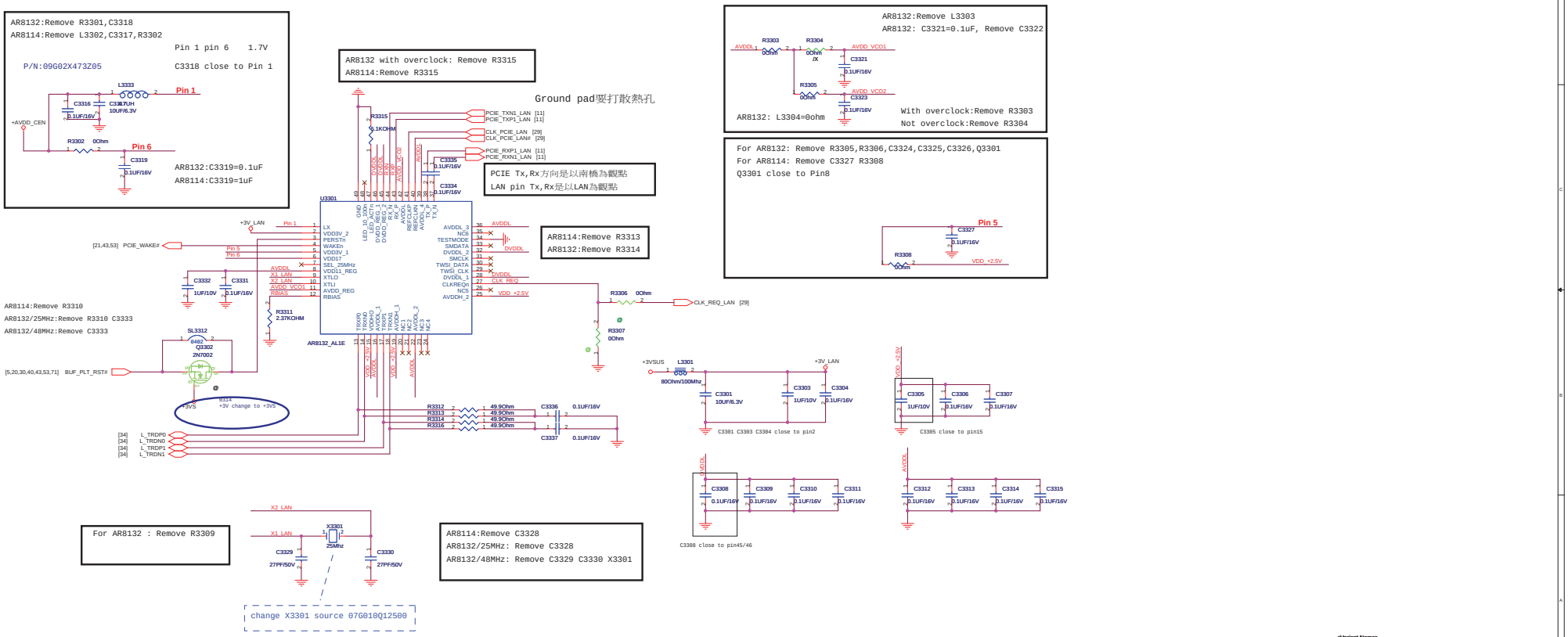
Title : *

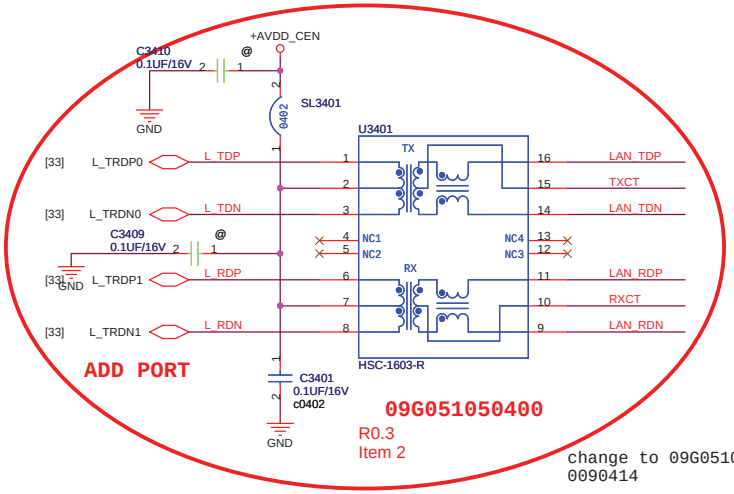
ASUSTeK COMPUTER INC

Engineer: Richard Lu

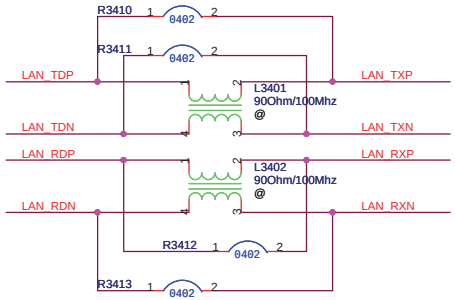
Size	Project Name	Rev
Custom	F5Z	2.05

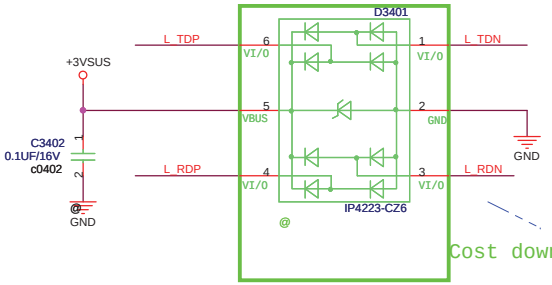
Date: Tuesday, May 26, 2009 Sheet 32 of 91





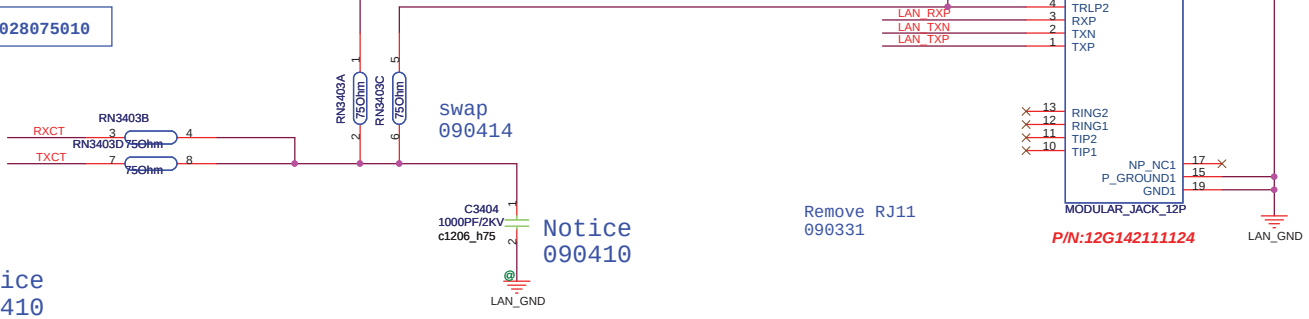
change to 09G0510010F9
0090414



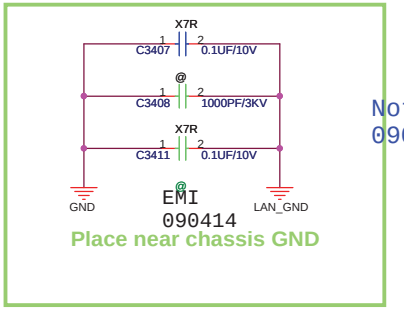


Cost down
07G028075010

For RJ-45/RJ-11



Remove RJ11
090331



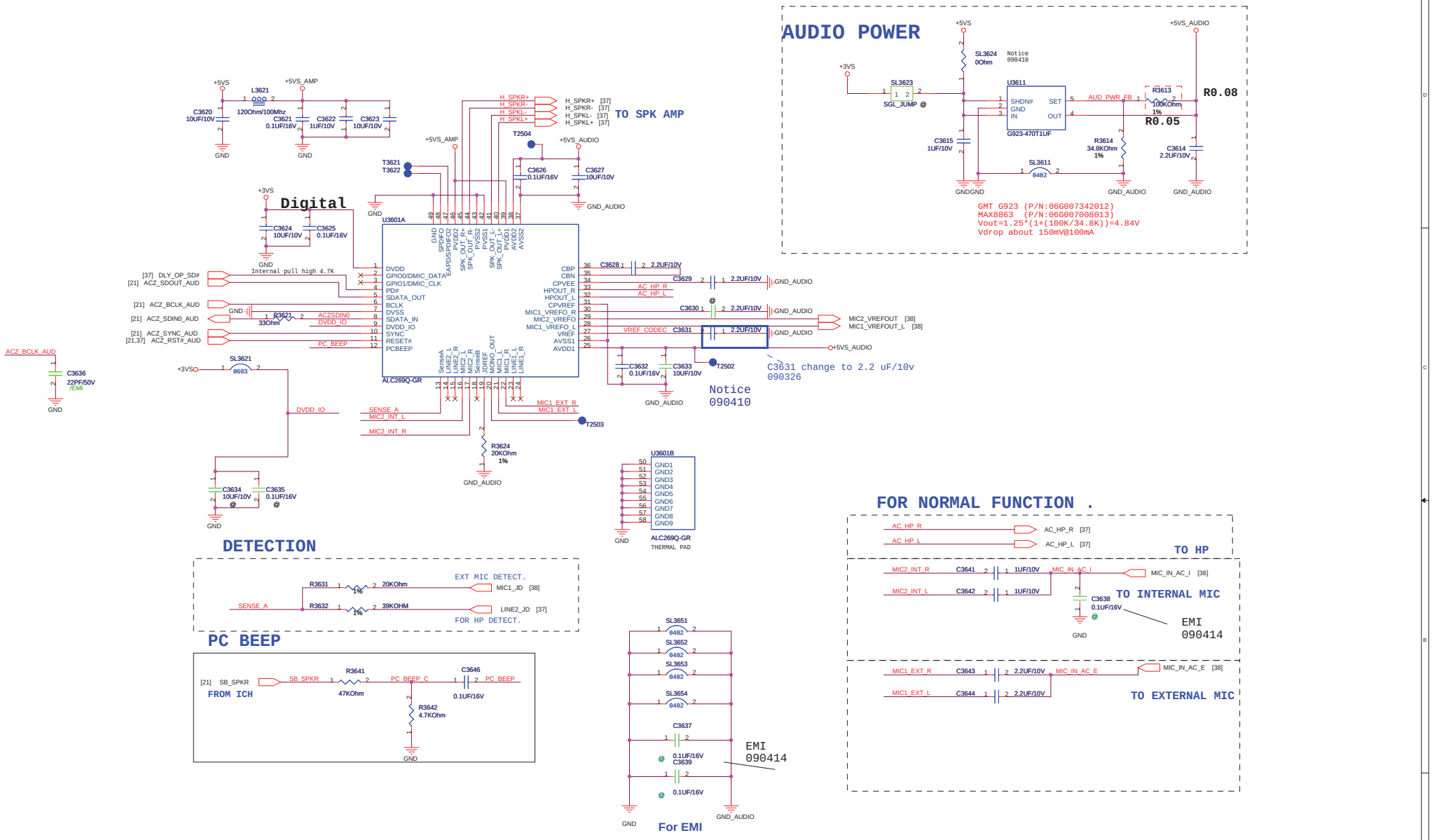
Notice
090410

<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN-RJ45	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Monday, June 01, 2009	Sheet 34 of 91	

<Variant Name>

ASUSTeK COMPUTER INC	Title : LAN-MDC	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 35 of 91	



<Variant Name>

ASUSTeK COMPUTER INC.

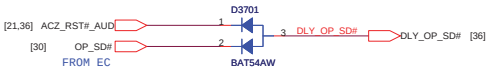
Title : CODEC-ALC662

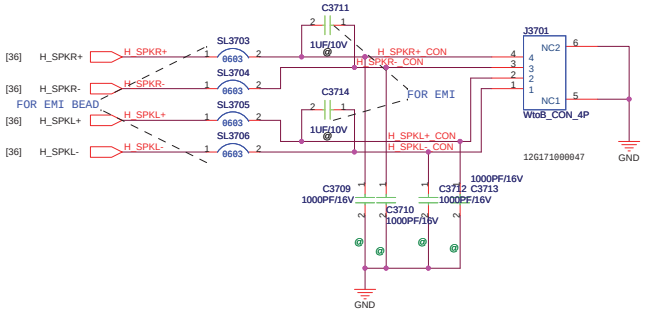
Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

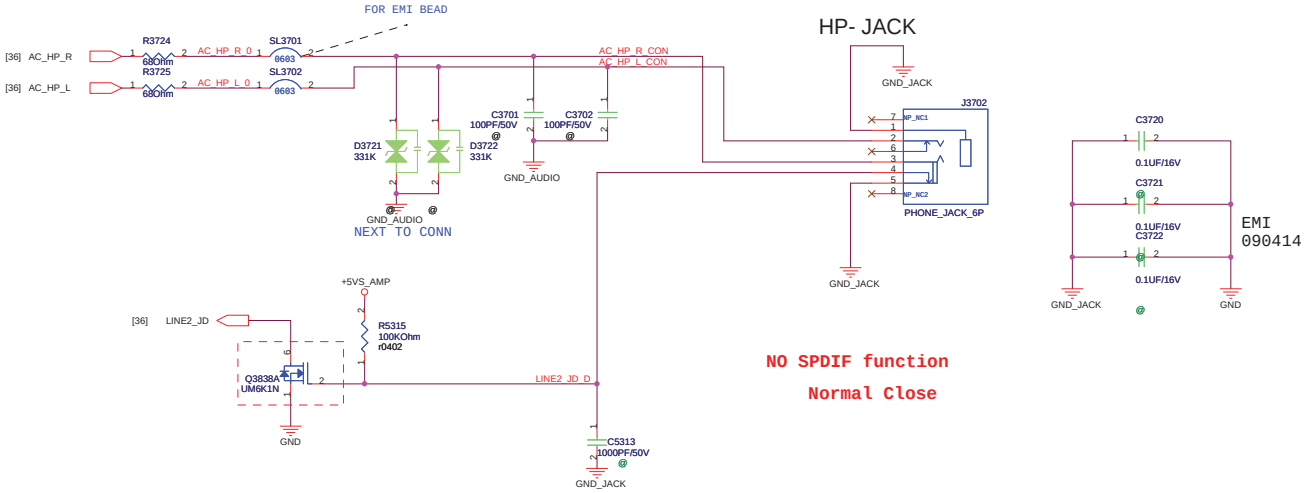
Date: Tuesday, May 26, 2009 Sheet 36 of 91

MUTE CONTROL

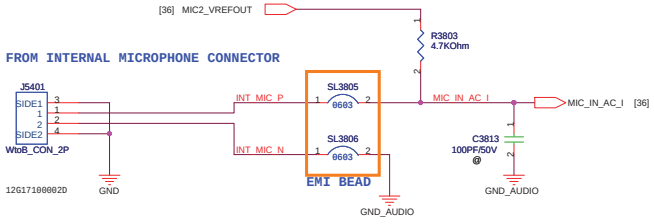




JACK_IN# or LINE2_JD depend on JACK's structure.
Suppose the fisrt pin should be contacted to GND while HP is plugged in.

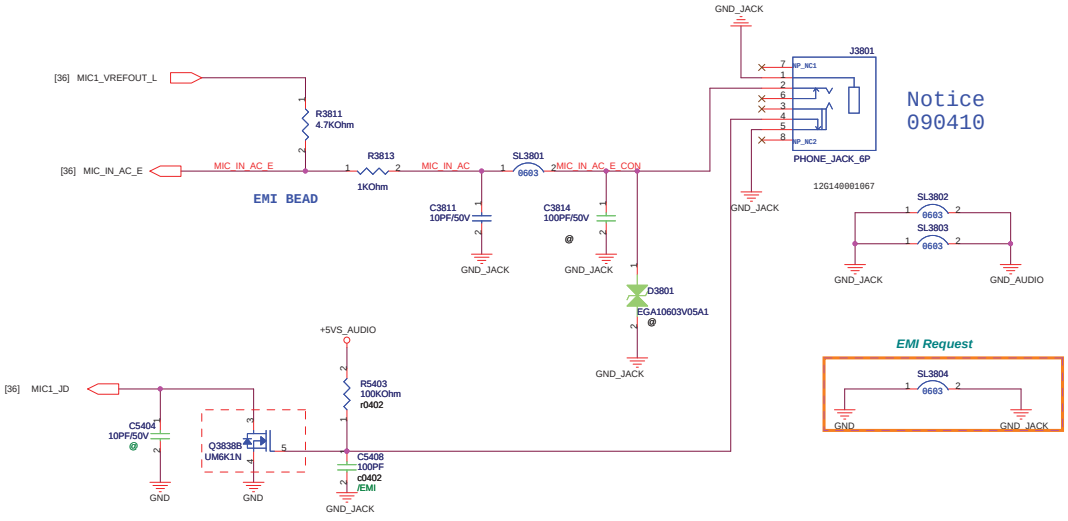


INTERNAL MICROPHONE



EXTERNAL MICROPHONE

Microphone In Jack



<Variant Name>

ASUSTeK COMPUTER INC.

Title : MIC-IN Jack

Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 38 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 39 of 91

Add +3vs 081228

AU6433-GLF:02G630001530
AU6433-GEF:02G630001521.
現在要求使用AU6433-GLF:02G630001530，
做bom以及線路要注意

Pin2 has internal pu 75K to +3V.

Close to chip

For AU6433 GLF : Stuff R4019(SL4008),
Remove R4012,R4013

1:For check
0:For no check (Default)

Remove Chock 2009/05/25

P/N:12G340003814

Fix MS Duo Adaptor short issue.
(SD_DAT1,SD_DAT2,XD_GND short,XD_CD# may be possible short)

For AU6433-GLF: No stuff All
For AU6433-GEF: Stuff Q4004,Q4005,Q4007,R4066.

IC side

CON side

<Variant Name>

Title : CB_AU-6371_JEL

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
C	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 40 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 41 of 91

<Variant Name>

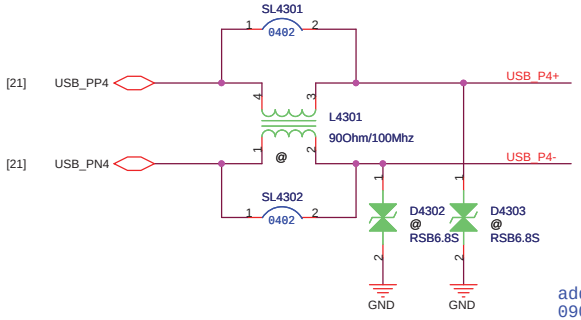
Title : *

ASUSTeK COMPUTER INC

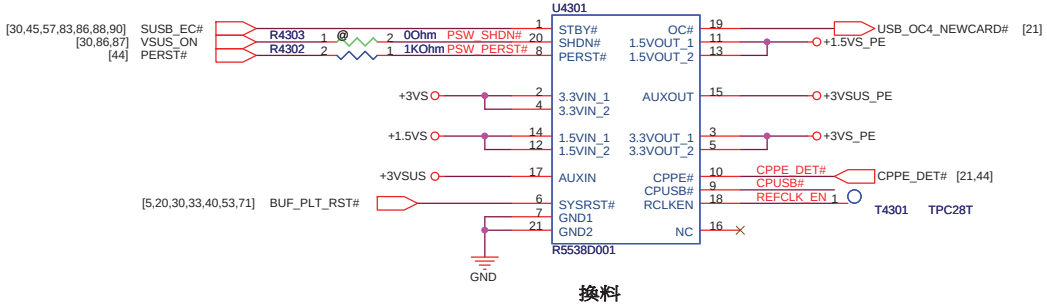
Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 42 of 91



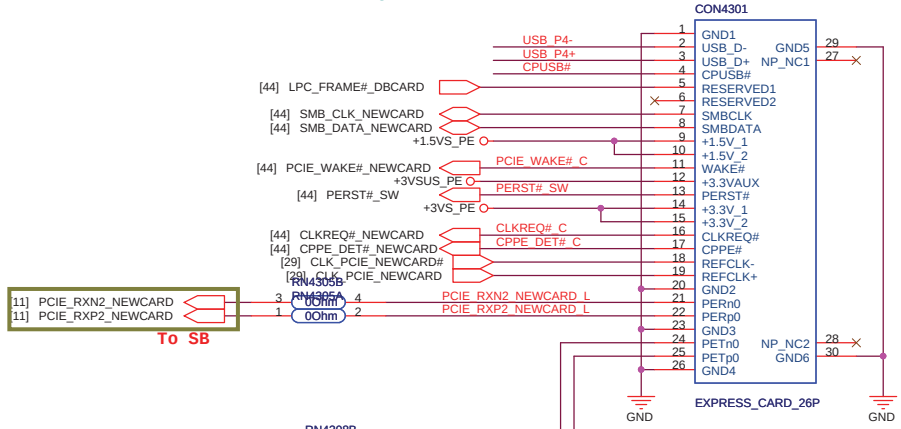
add RN4301, 預留L4301,
090331



換料

!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

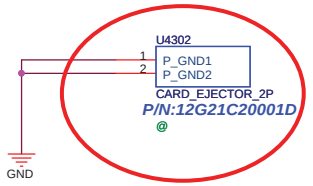
NewCard Header



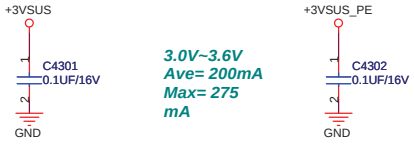
PN:12G161300261

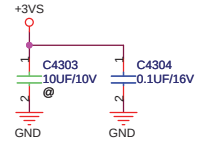
R2.0 080402
Un-mount U4302 (Since it is not SMT component)

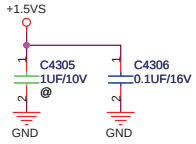
080216 R1.1
Add Resistor



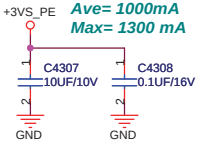
Remove U4302.
090406



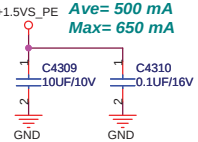


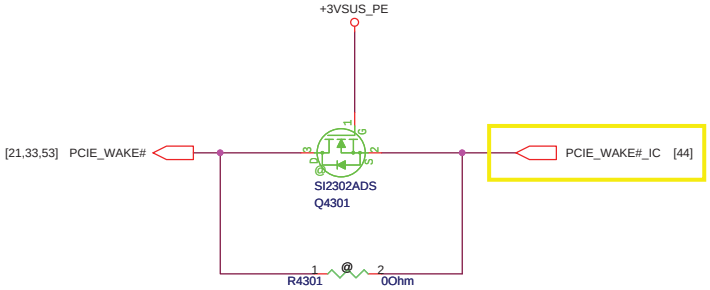


3.0V~3.6V
Ave= 1000mA
Max= 1300 mA



1.35V~1.65V
Ave= 500 mA
Max= 650 mA



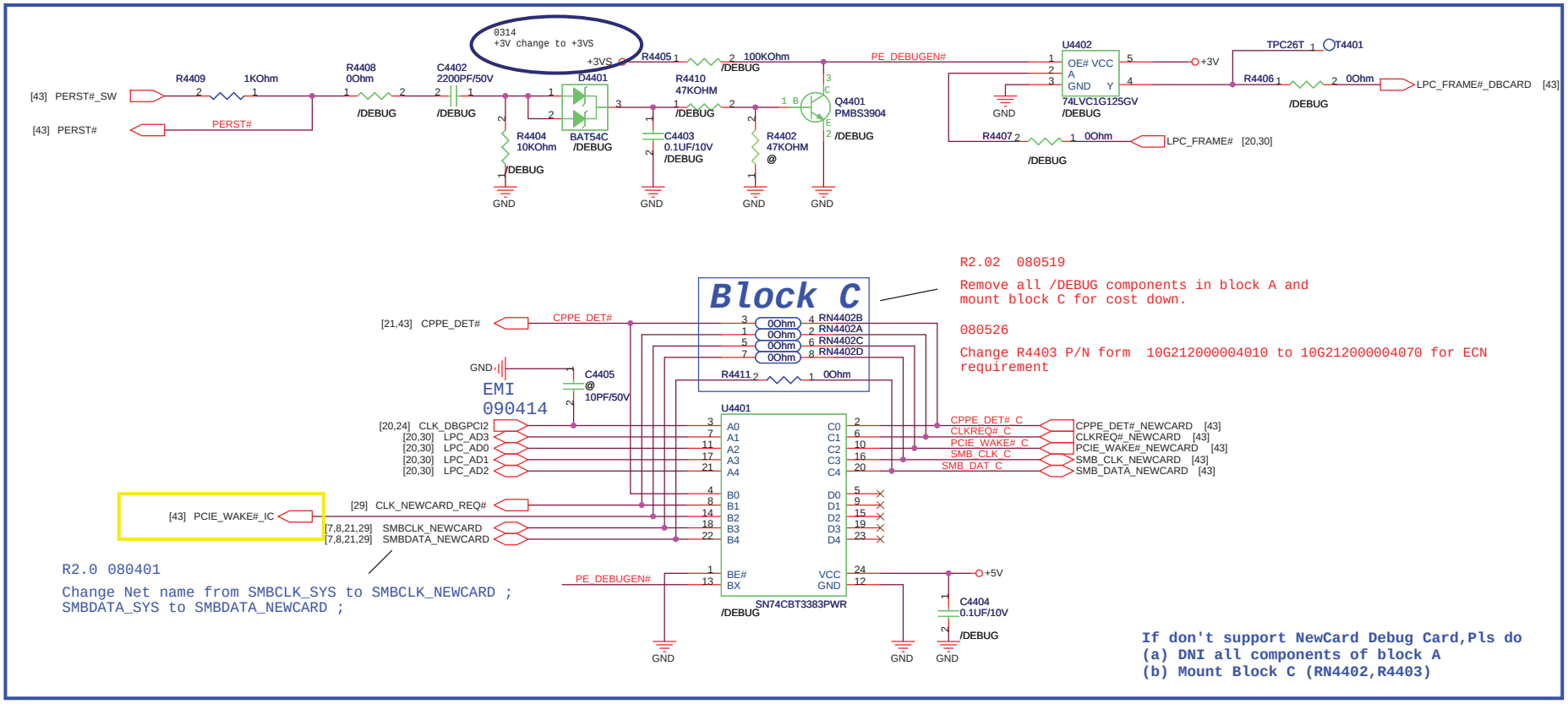


RemoveNew Card REFCLK_EN control part
090331

<variant_name>

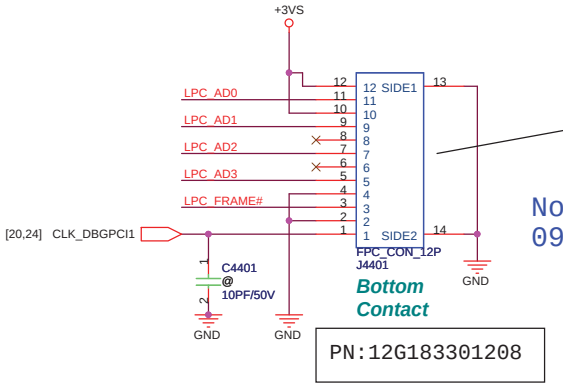
Title : NEWCARD
ASUSTeK COMPUTER INC
Engineer: Richard_Lu
Size: Custom
Project Name: F5Z
Rev: 2.05
Date: Tuesday, May 26, 2009
Sheet 43 of 91

Block A



For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.



R2.04
Un-mount J4401 for cost down

Notice
090410

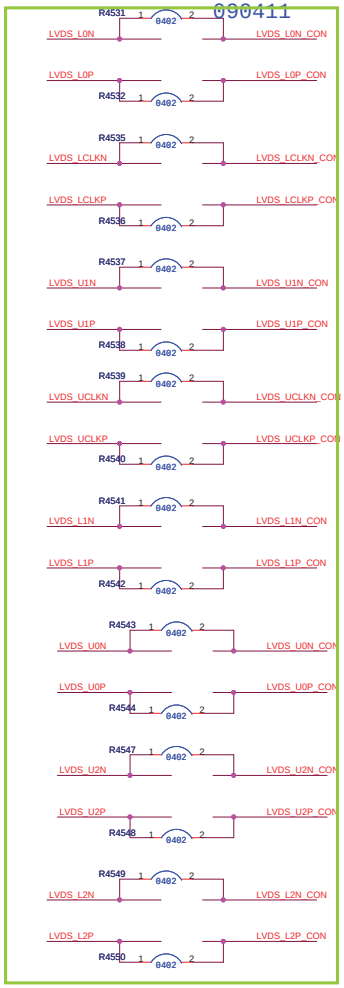
R2.05
Change RN4401 from 100ohm to 100pF capacitance. The capacitance with modification of RNX3001 is used to fix the LAD and SERIRQ signals coupling issue. However, the LPC debug board EEROM over-write function is not support now.

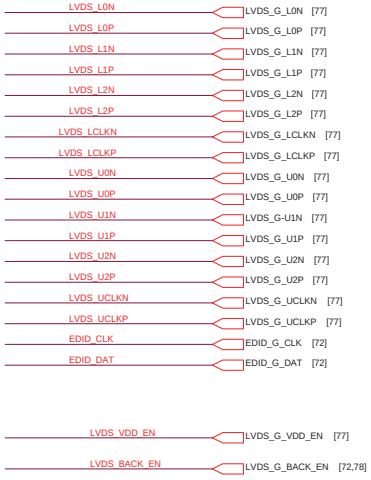
<Variant Name>

ASUSTeK COMPUTER INC	Title : DEBUG	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 44 of 91	

layoutguide notic those SL colay with chock
090411

M92-M2

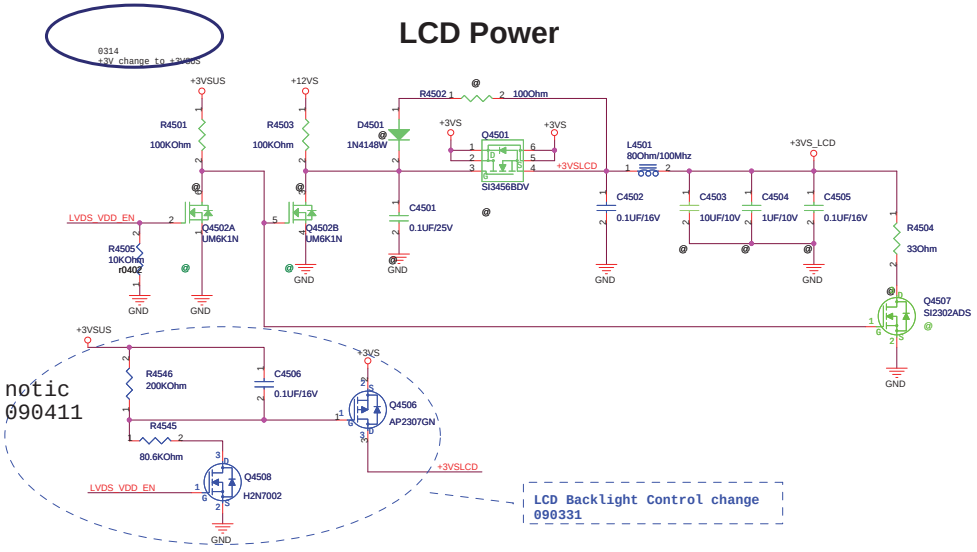




Remove Bead 2005/05/25

LCD Backlight Control

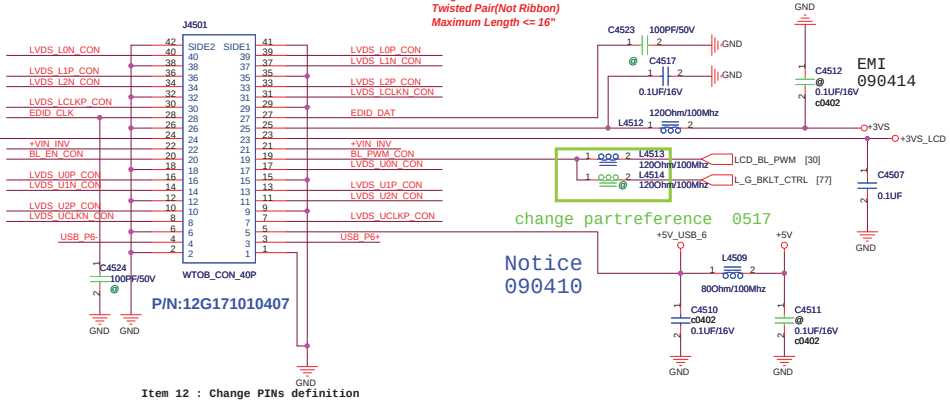
LCD Power



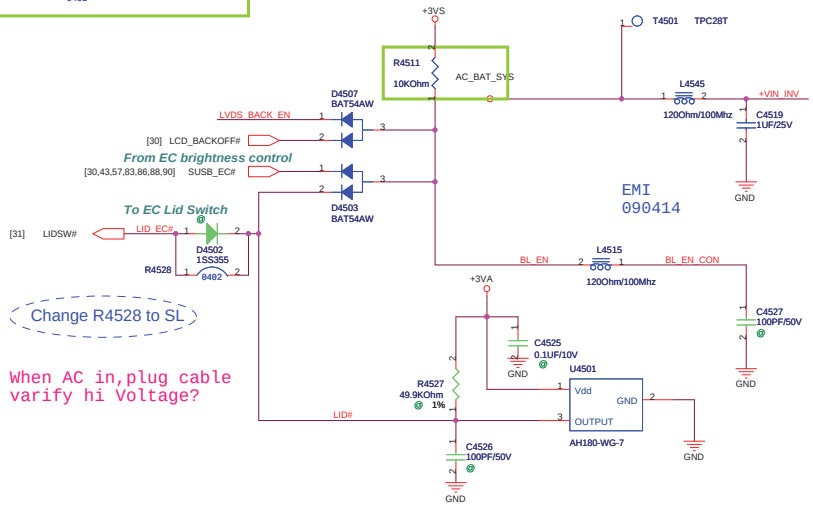
LCD Backlight Control change 090331

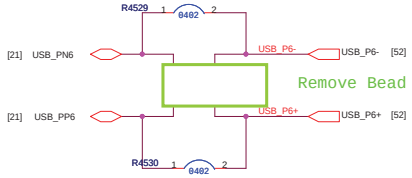
LCD LVDS/Inverter/CCD conn.

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



Item 12 : Change PINs definition

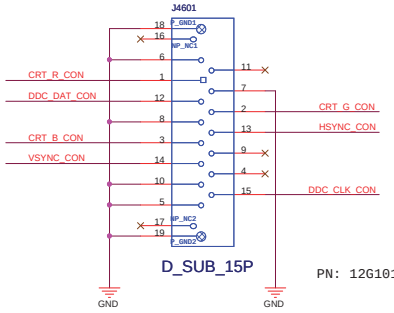




change SL
090411

<Variant Name>

Title : LVDS & INVERTER
ASUSTeK COMPUTER INC.
Engineer: Richard_Lu
Size: C | Project Name: F5Z | Rev: 2.05
Date: Friday, May 29, 2009 | Sheet 45 of 91



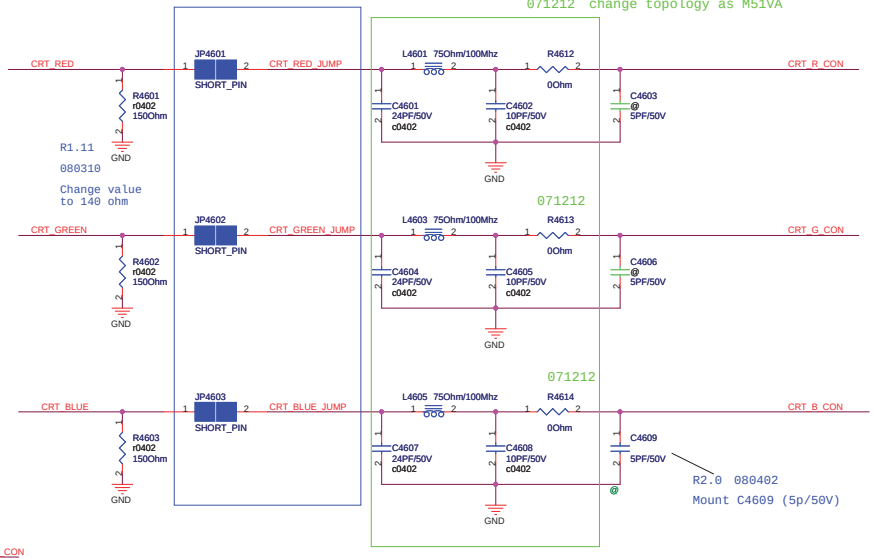
PN: 12G10110915K

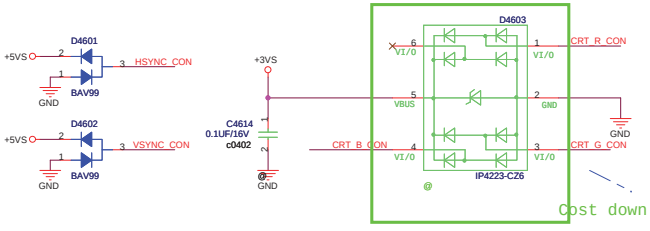
PLACE ESD Diodes near
VGA port

071204 Add Jump

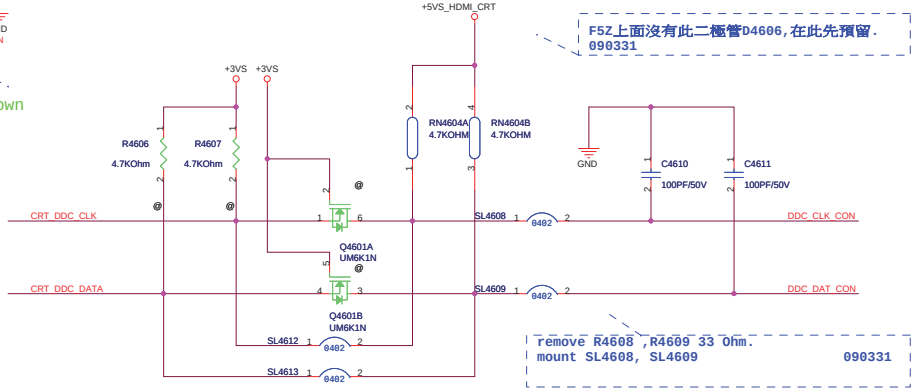
071113

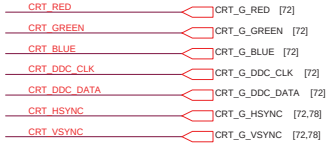
071212 change topology as M51VA

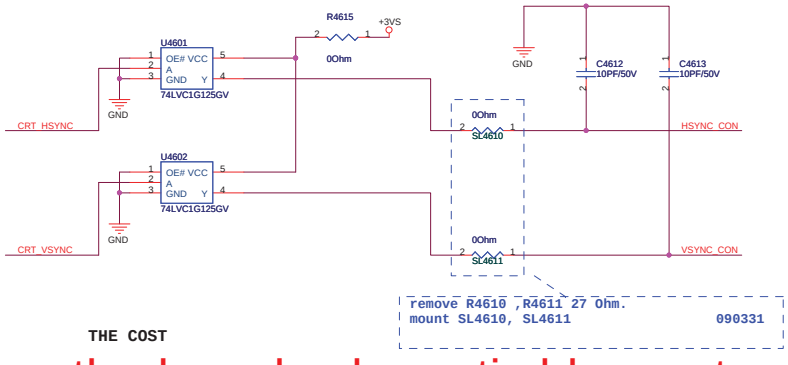




Notice change P/N
090410







THE COST

<Variant Name>

Title : CRT

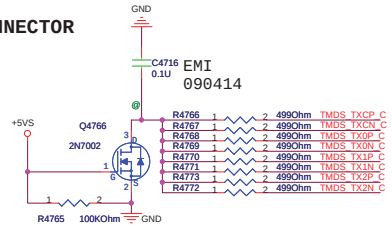
ASUSTeK COMPUTER INC.

Engineer: Xinghua_chen

Size	Project Name	Rev
C	F83T	2.0

Date: Friday, May 29, 2009 Sheet 46 of 91

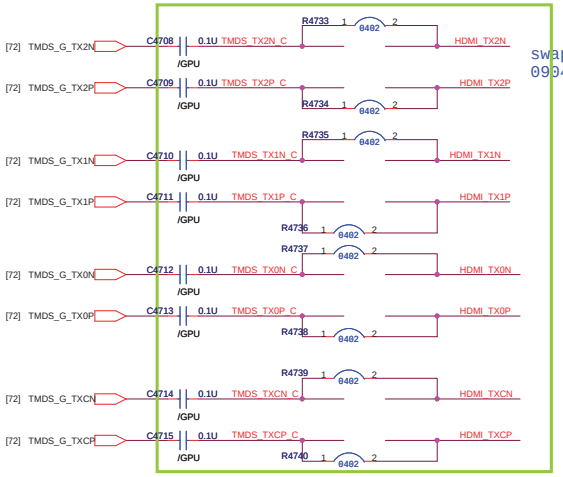
Close to CONNECTOR



不建議換成排阻.
090406

Close to CONNECTOR

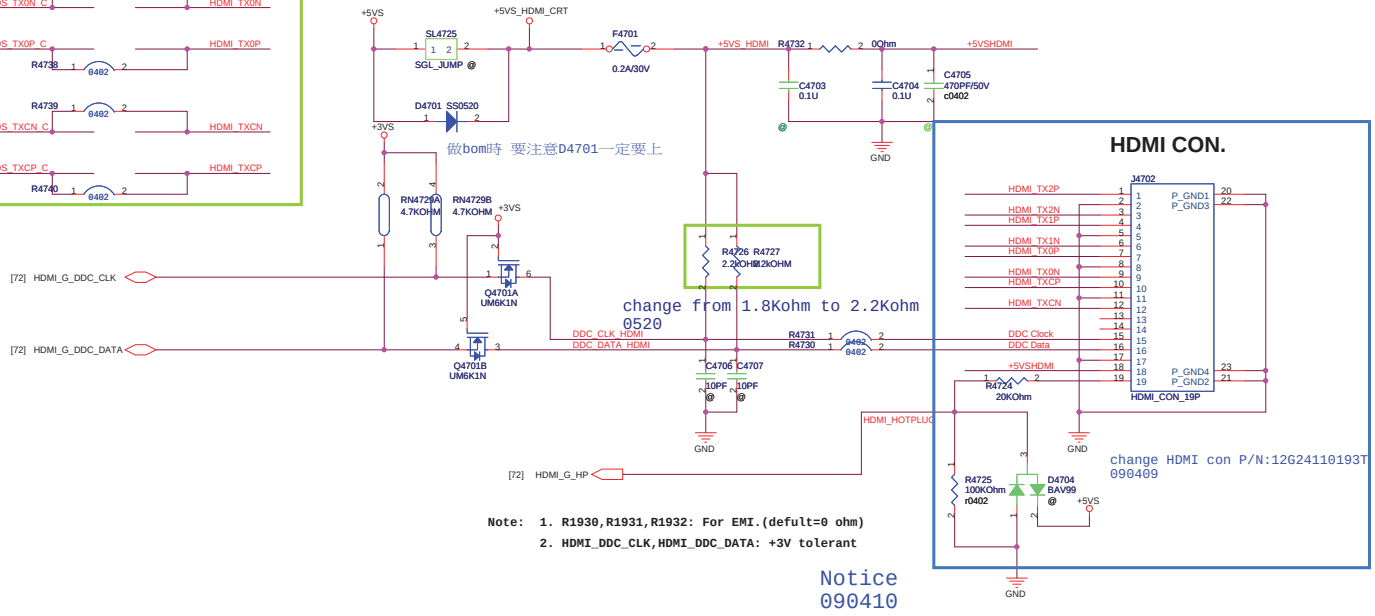
Notice
090410



swap
090414

Remove Bead

Notice
090410



Note: 1. R1930,R1931,R1932: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +3V tolerant

Notice
090410

ASUSTeK COMPUTER INC.	Title : HDMI	
	Engineer: Kuten Hsu	
Size: C	Project Name: F5Z	Rev: 2.05
Date: Wednesday, May 27, 2009	Sheet 47 of 91	

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

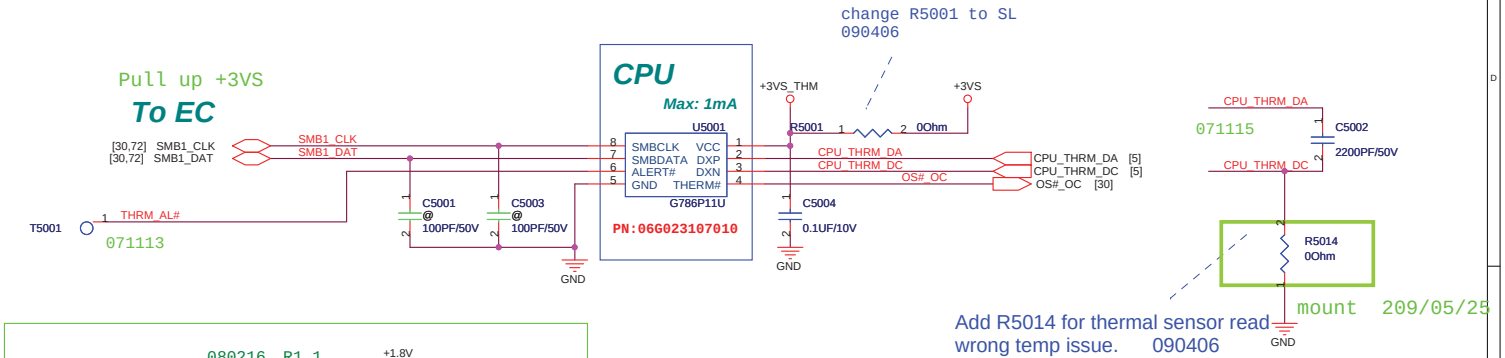
Size	Project Name	Rev
Custom	F5Z	2.05

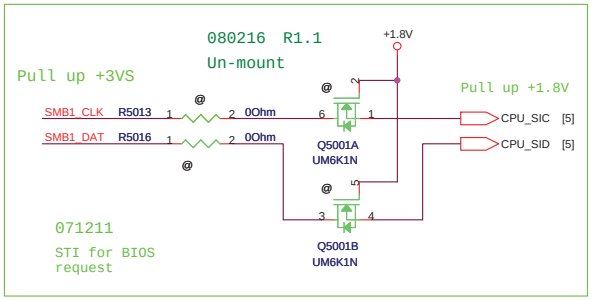
Date: Tuesday, May 26, 2009 Sheet 48 of 91

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Richard Lu	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 49 of 91	

Thermal Sensor



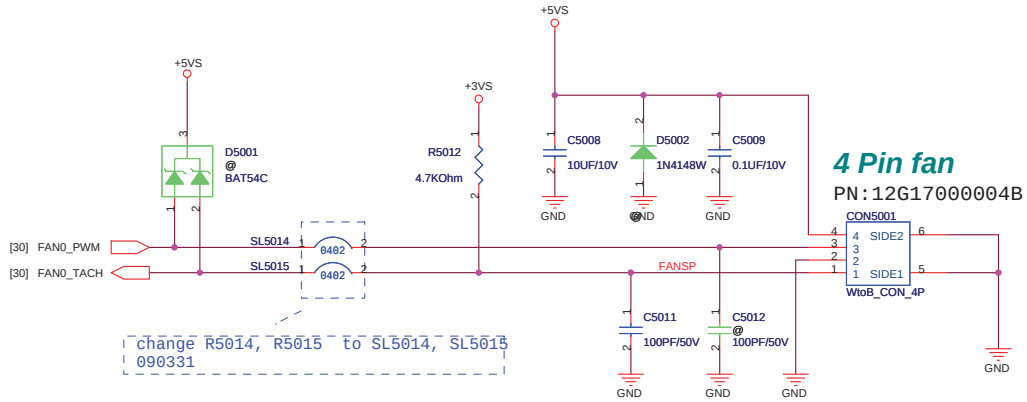


Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



<Variant Name>

Title : THER SENSOR & FAN

ASUSTeK COMPUTER INC

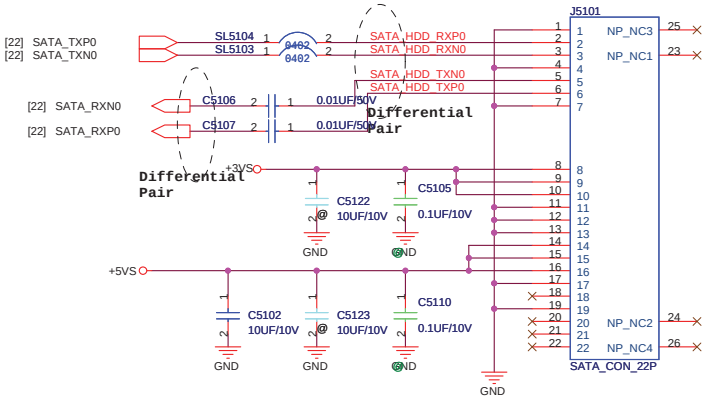
Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 50 of 91

SATA HDD

SATA HDD CON

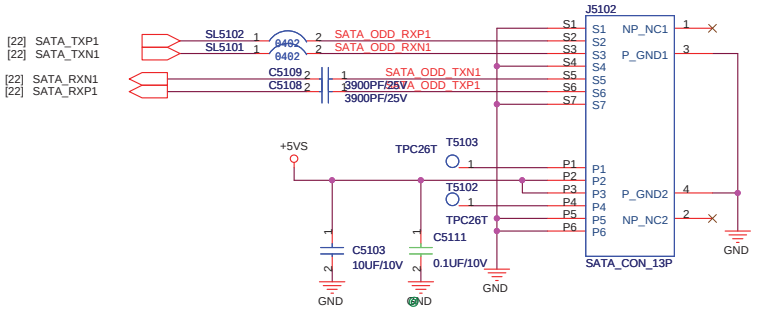


P/N:12G15200022G

MLCC 4700PF/25V (0402)X7R 10%
11G232147212360 Design IP

MLCC 0.1UF/10V (0402) X7R 10%
11G232110416360
比較一下價格

ODD



P/N:12G15100013J

<Variant Name>

Title : HDD & CD-ROM

ASUSTeK COMPUTER INC

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 51 of 91

071119 change common choke and R P/N

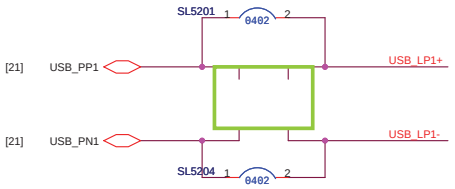
080213 R1.1
Change D5201 , D5204 , D5206 , D5208 footprint

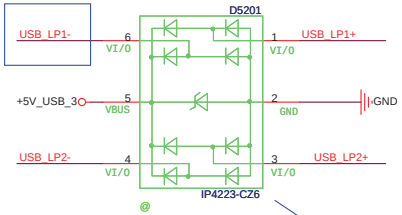
080125 R1.1
Change the USB Varisitor from EGA10603V05A1 to AZC099-04S

080215 R1.1
SWAP

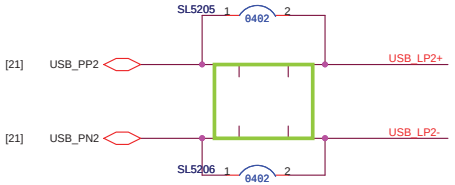
080218 R1.1
Change PN From 07G014075600 to 07G014075310

Change all MOS with ESD part

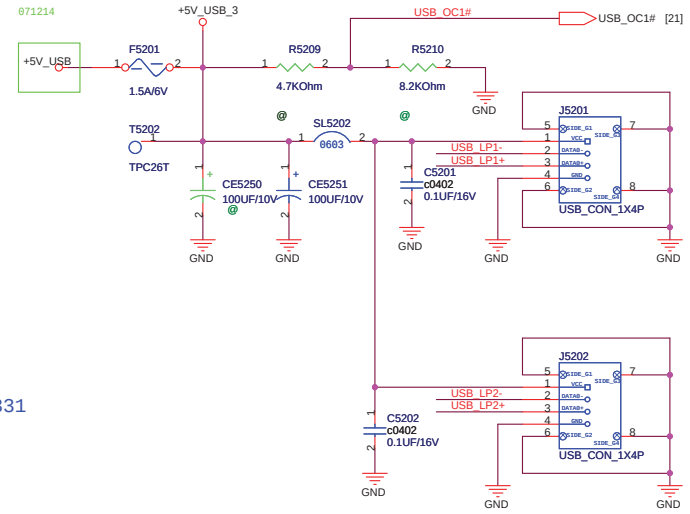




07G028075010為建議用料
已經更換. 090331

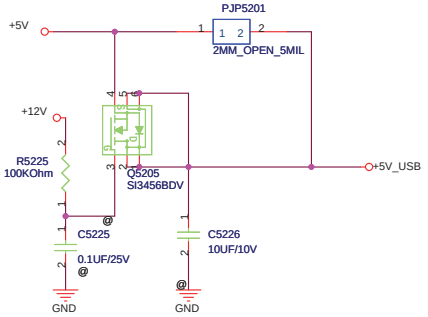


Remove Bead 2005/05/25

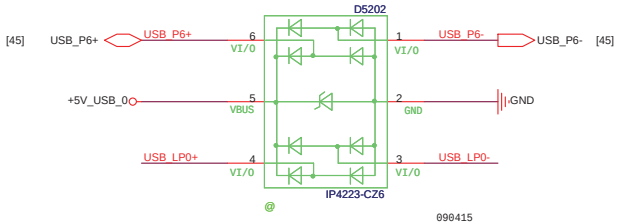


P/N:12G130011045

old:usb_1x4p_4hold_sun_lf3
new:nb_usb_1x4p_4hold_su_lf2

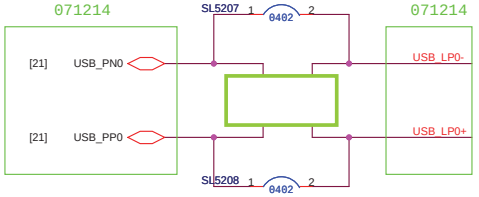


預留USB OC function 090406



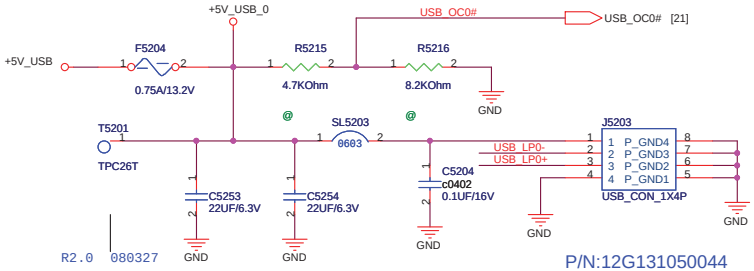
090415

swap 071214



swap 071214

SWAP
090417



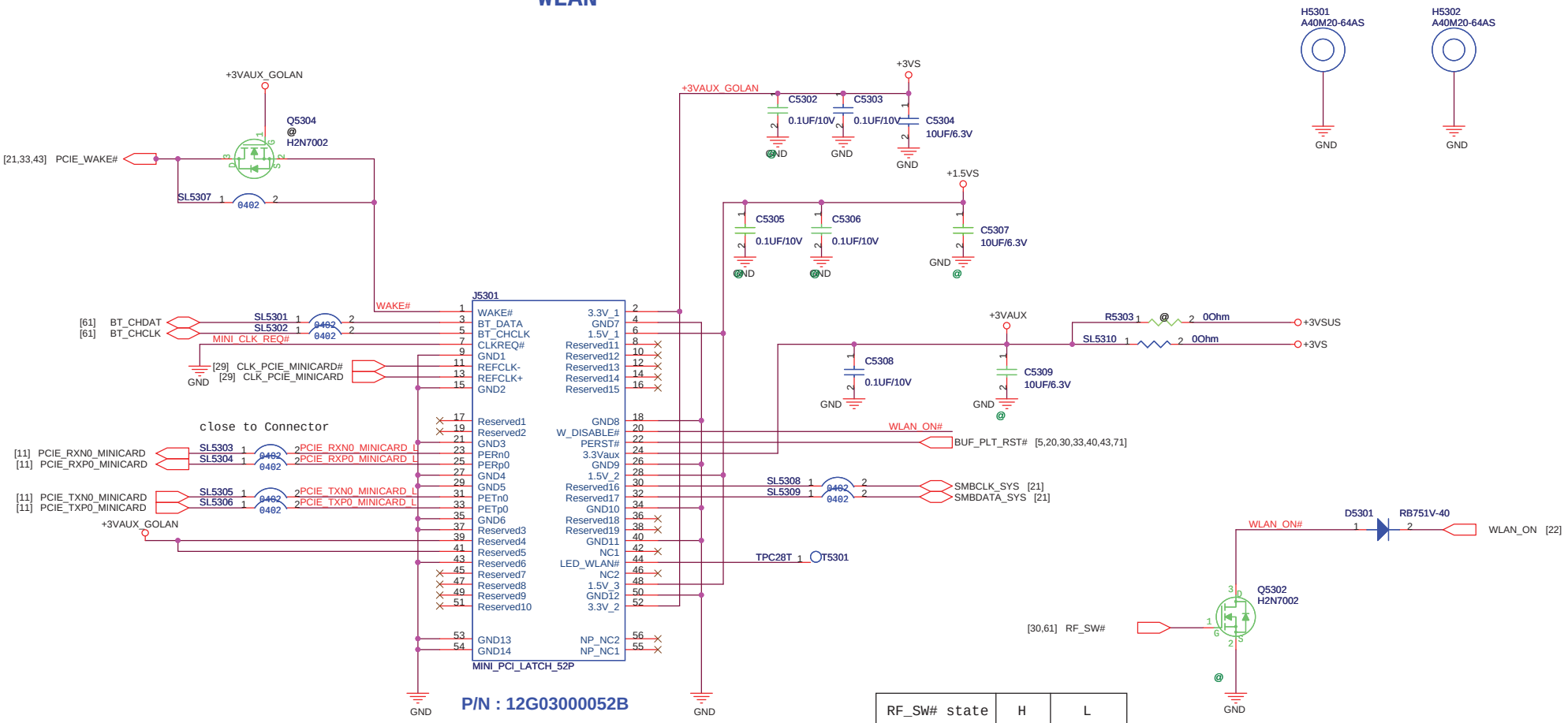
R2.0 080327
Add test point for factory ICT test

P/N:12G131050044

<Variant Name>

ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 52 of 91	

WLAN



P/N : 12G03000052B

RF_SW# state	H	L
WLAN state	Off	On

<Variant Name>

ASUSTeK COMPUTER INC

Title : MINICARD

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.0

Date: Friday, May 29, 2009 Sheet 53 of 91

<Variant Name>

ASUSTeK COMPUTER INC	Title : *
	Engineer: Richard Lu
Size: A	Project Name: F5Z
Rev: 2.05	
Date: Tuesday, May 26, 2009	Sheet 54 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
A	F5Z	2.05

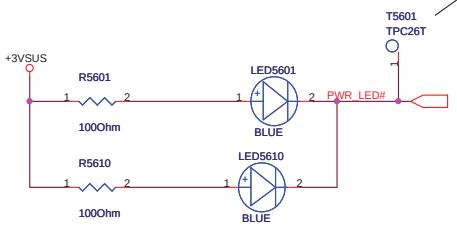
Date: Tuesday, May 26, 2009 Sheet 55 of 91

LED

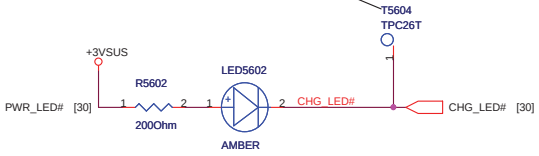
R2.0 080327

Add test point for factory ICT test

For POWER LED

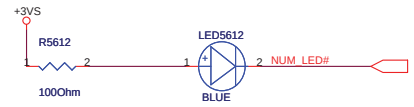


BATTERY LED



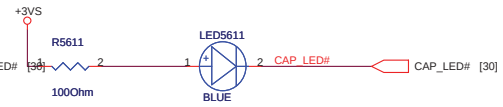
Num Lock

071122



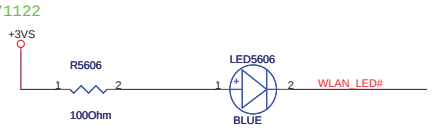
Cap Lock

071122



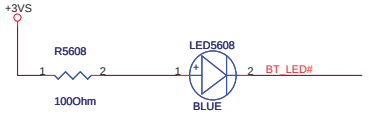
WireLess LED

071122



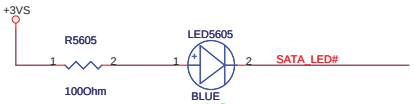
BT LED

071122



SATA/IDE LED

071122 071127

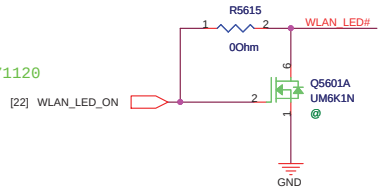


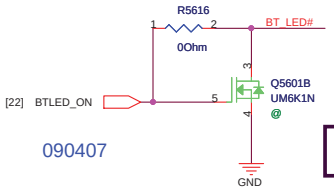
delete D5601

071127

From SB GPIO

071120





090407

Change all LED for 5mA

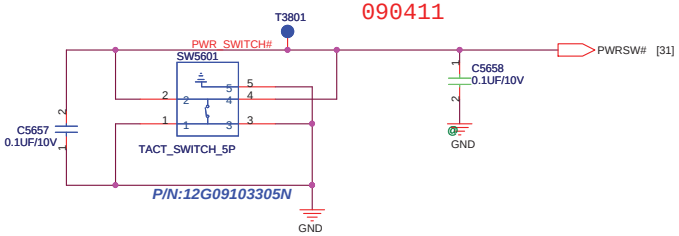
Change all MOS with ESD part

F5Z SWITCH CIRCUIT

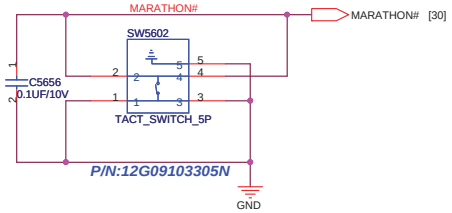
Move SW from P32 to P56

Power SW.

Remove R5656
090411



MARATHON#



<Variant Name>

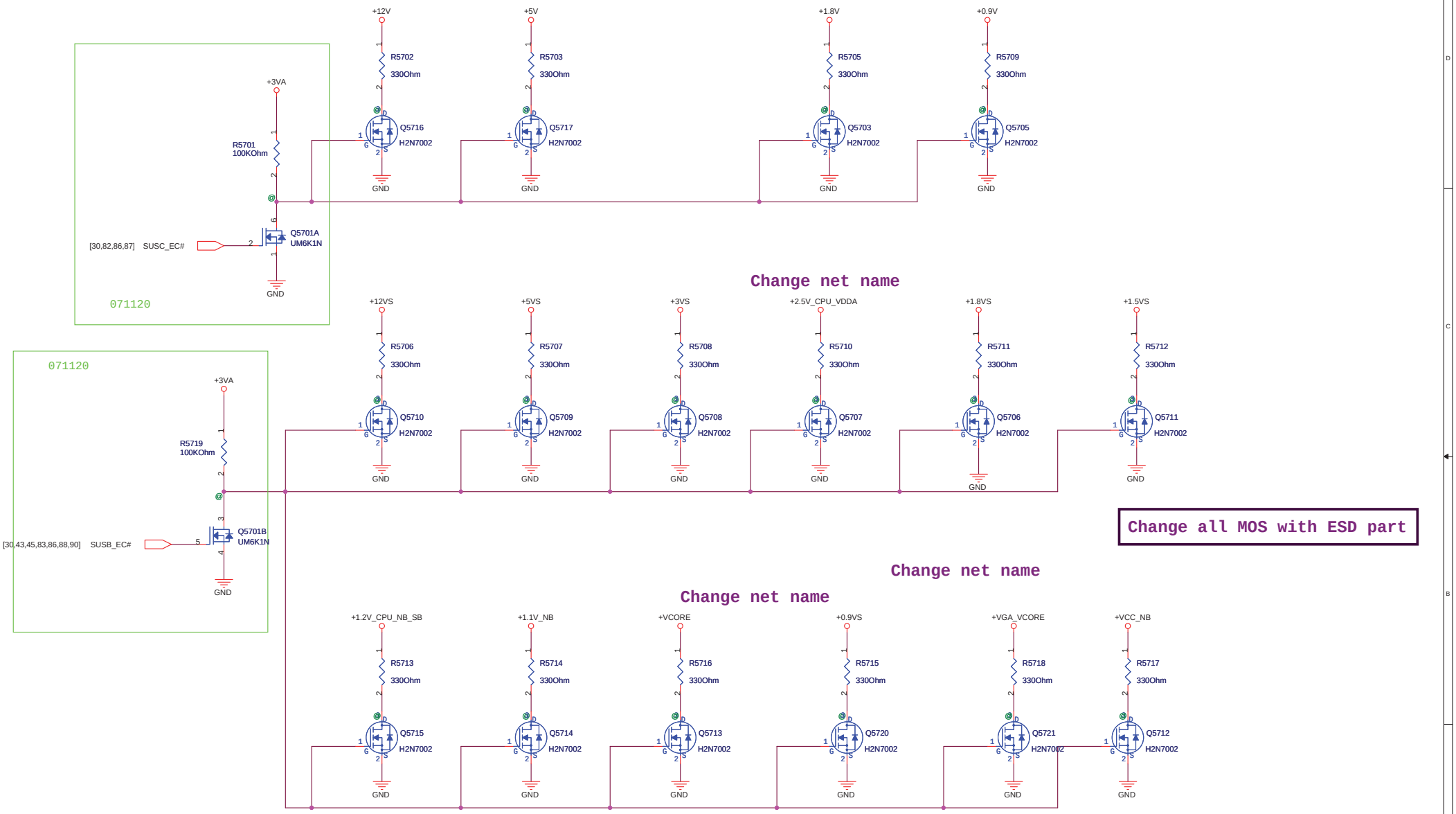
Title : LED/PWR SWICH

ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.0

Date: Wednesday, May 27, 2009 Sheet 56 of 91



<Variant Name>

Title : DISCHARGE CKT

ASUSTeK COMPUTER INC

Engineer: Xinghua_chen

Size	Project Name	Rev
Custom	F83T	2.0

Date: Wednesday, May 27, 2009 Sheet 57 of 91

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Richard_Lu	
Size: Custom	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 58 of 91	

<Variant Name>

ASUSTeK COMPUTER INC	Title : *	
	Engineer: Richard Lu	
Size: A	Project Name: F5Z	Rev: 2.05
Date: Tuesday, May 26, 2009	Sheet 59 of 91	

BATTERY

cahnge PL->L,PT->T,PC->C

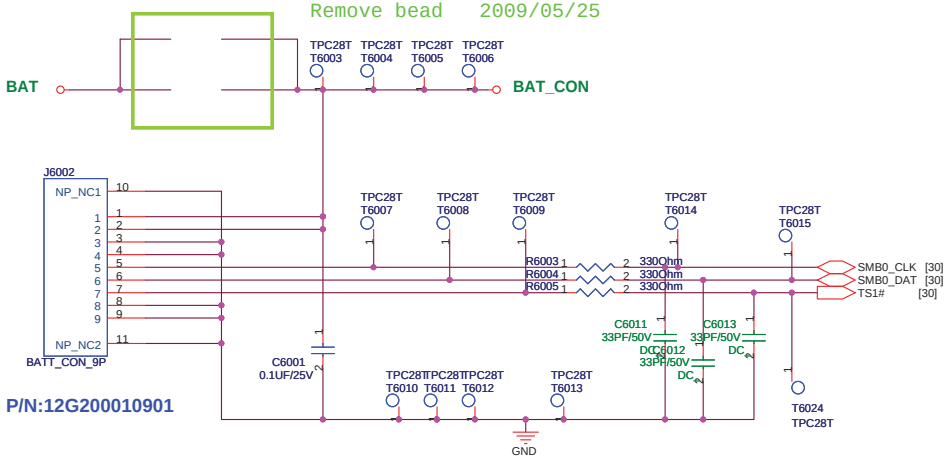
071120

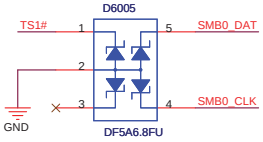
Removen JP

Remove bead 2009/05/25

change footprint

071203

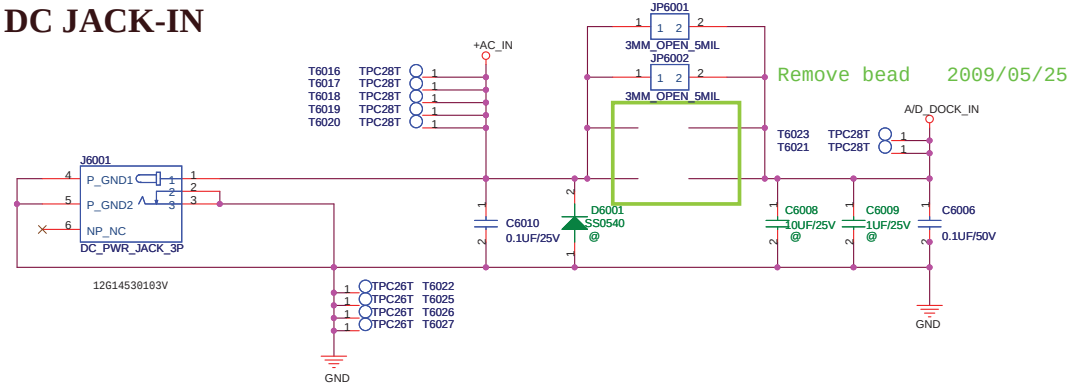




Add for AC Adapter protect

Adaptor IN

DC JACK-IN



<Variant Name>

Title : DC_Jack & BAT Con

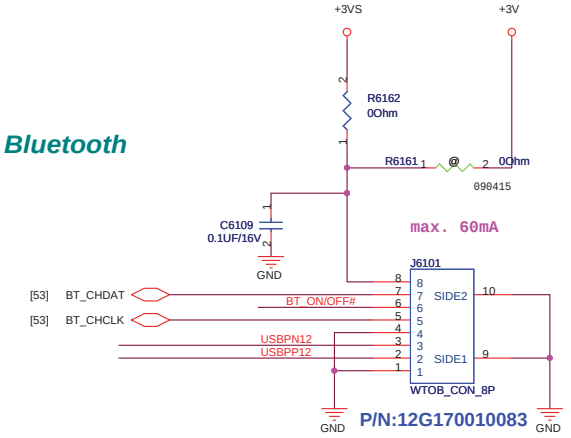
ASUSTeK COMPUTER INC

Engineer: Richard_Lu

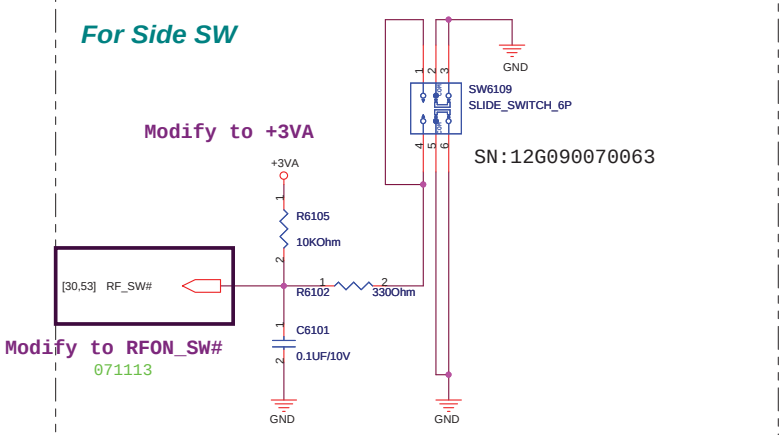
Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 60 of 91

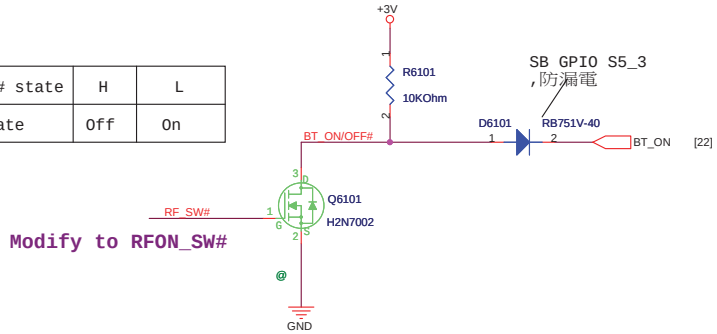
For Bluetooth

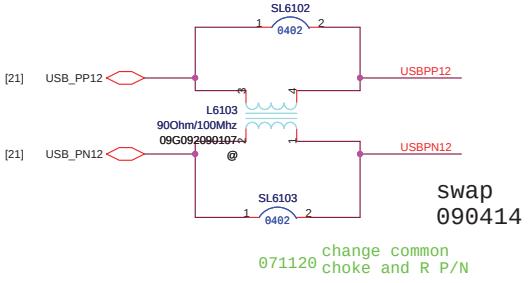


For Side SW

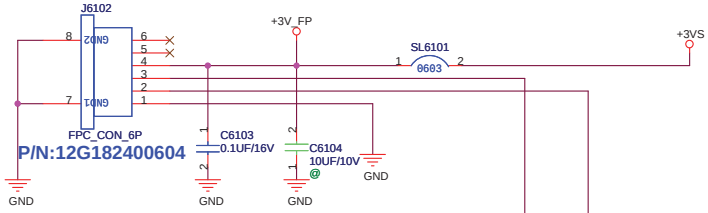


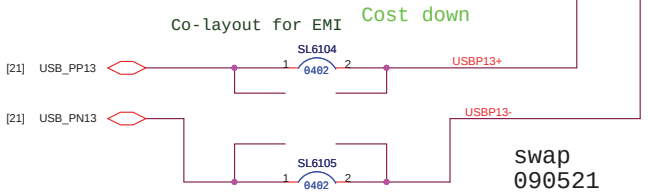
RF_SW# state	H	L
BT state	Off	On



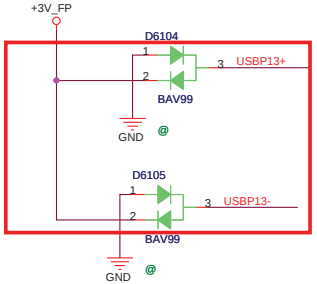


Fingerprint Conn.





optional，先上測試功能



<Variant Name>

Title : BT & Slide SW

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F83T	2.05

Date: Friday, May 29, 2009 Sheet 61 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 62 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 63 of 91

<Variant Name>

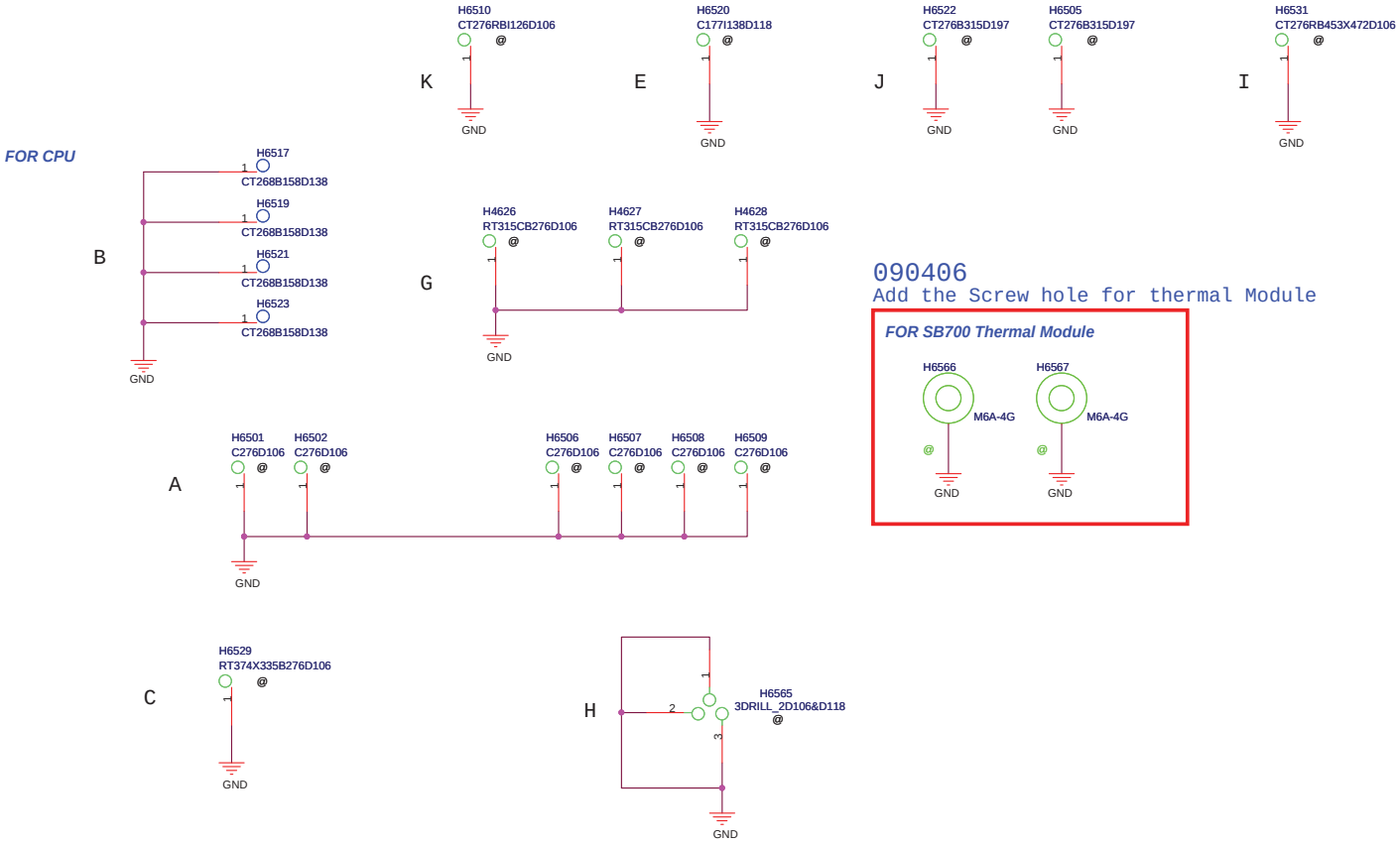
Title : TUN

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 64 of 91

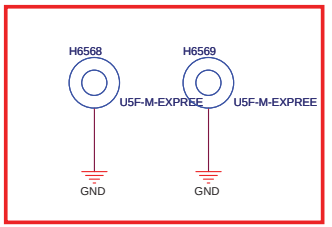


090406

Add the Screw hole for thermal Module

090406

Add the Nut for GPU thermal Module



change to P/N:13GN9980M090-1 for high limit

<Variant Name>

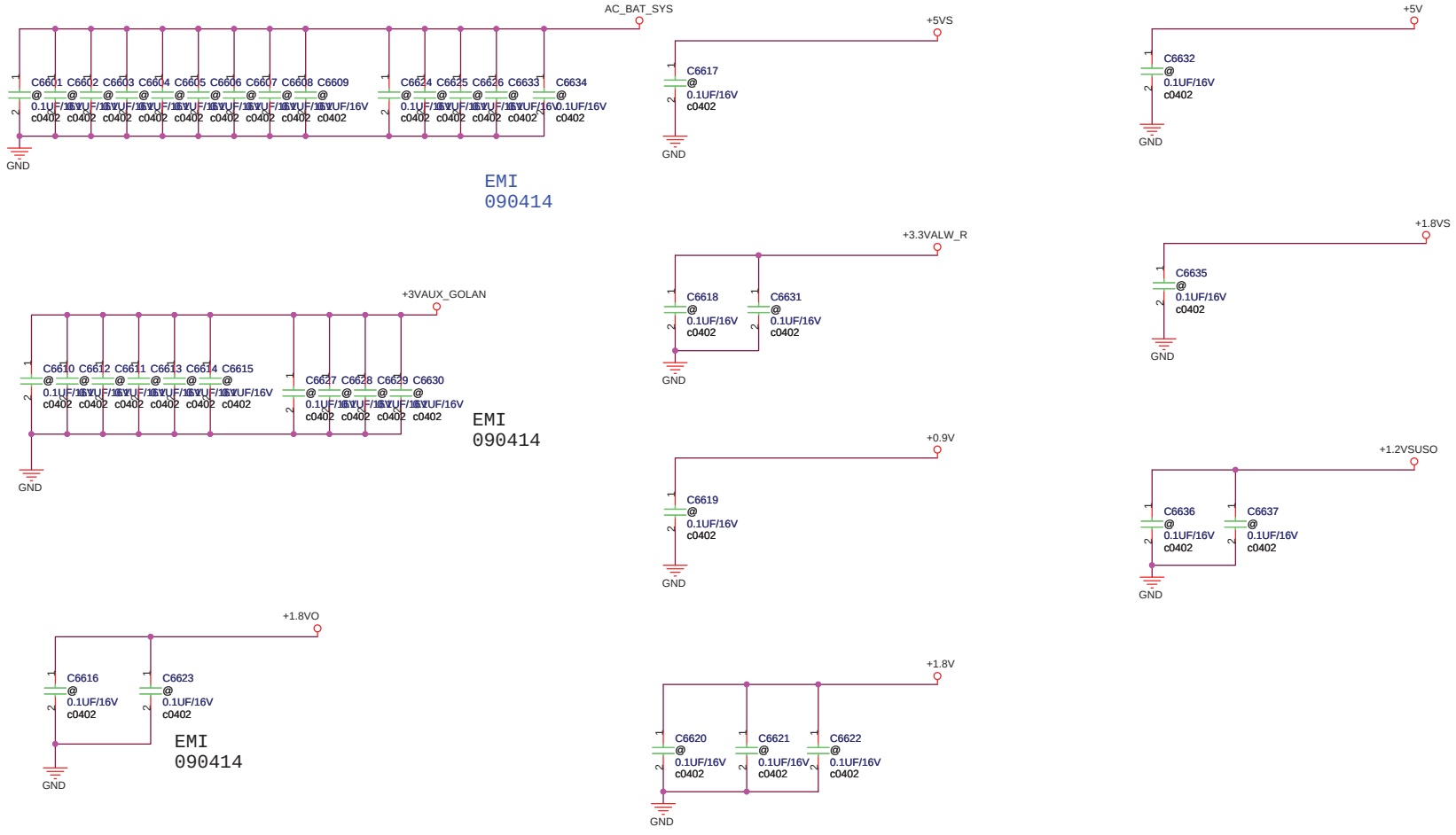
Title : Screw Hole

ASUSTeK COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Friday, May 29, 2009 Sheet 65 of 91



<Variant Name>

ASUSTeK COMPUTER INC

Title : EMI

Engineer: Richard_Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 66 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
B	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 67 of 91

<Variant Name>

Title : *

ASUSTeK COMPUTER INC

Engineer: Richard Lu

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 68 of 91

1,Vram data swap. 090327

2,修改VGA_CORE 電壓，Boot 電壓為1.2V. 090327

3, Page72 add a resister which connect between
XTALIN and XTALOUT when a 27MHz crystal is used. 090329

4, SWAP VRAM data Group4 and Group5 090330

5,Audio AVDD 預留 +3VS 090330

6, Add RN4301, 預留L4301. 090331

7,remove R4610 ,R4611 27 Ohm.(EMI), remove R4608 ,R4609 33 Ohm.
mount SL4608, SL4609 ,mount SL4610, SL4611 090331

8,LCD Backlight Control change 090331

9,Remove RJ11 090331

11,SB710 的晶振換成F80系列的32.768KHz的晶振.
網卡的25MHz的晶振換成料號為07G010Q12500. 090331

12, U4301 pin 18 REFCLKEN NC, remove part 090331

13,Change the ClkGen to RTM880T-797 090331

14, AU6433-GLF mount R4007 090331

15,CLK_REQ_LAN is OD ,add R2003 pull high. 090401

17,change power cap PCE8701 & PCE8702 090401

18,change the Screw Hole,Add the Nut for GPU thermal Module 090406

19,Modify the NB & SB power cap 090406

20,Swap the cap pack in page31 090406

21,changeR4726,R4727 from 1.8Kohm to 2.2Kohm 090520

22.Add buffer U4601,U4602 090520

24.Change R4511 to 10Kohm,R7870 to 2.2Kohm 090520

25.Add R2037 for safety 090520

28.Remove L6003,L6004,L6005,L6006 090525

29. Add 10uF cap C7549 090525

30.Remove L4001, L4502, L4506, L4508, L4511, L4503, L4507, L4510, L4504,
L4505, L6104, L5201, L5202, L5204, L4704, L4705, L4706, L4707 090525

31.Mount R5014, R7207 090525

32.預留 X7201, C7220, C7219, R7214, R7257 090525

33.Remove NUT for SB 090525

34.Change X2201 P/N:07G010Q12500 090525

35.Change R0403, R0404 from 15ohm to 1Kohm 090525

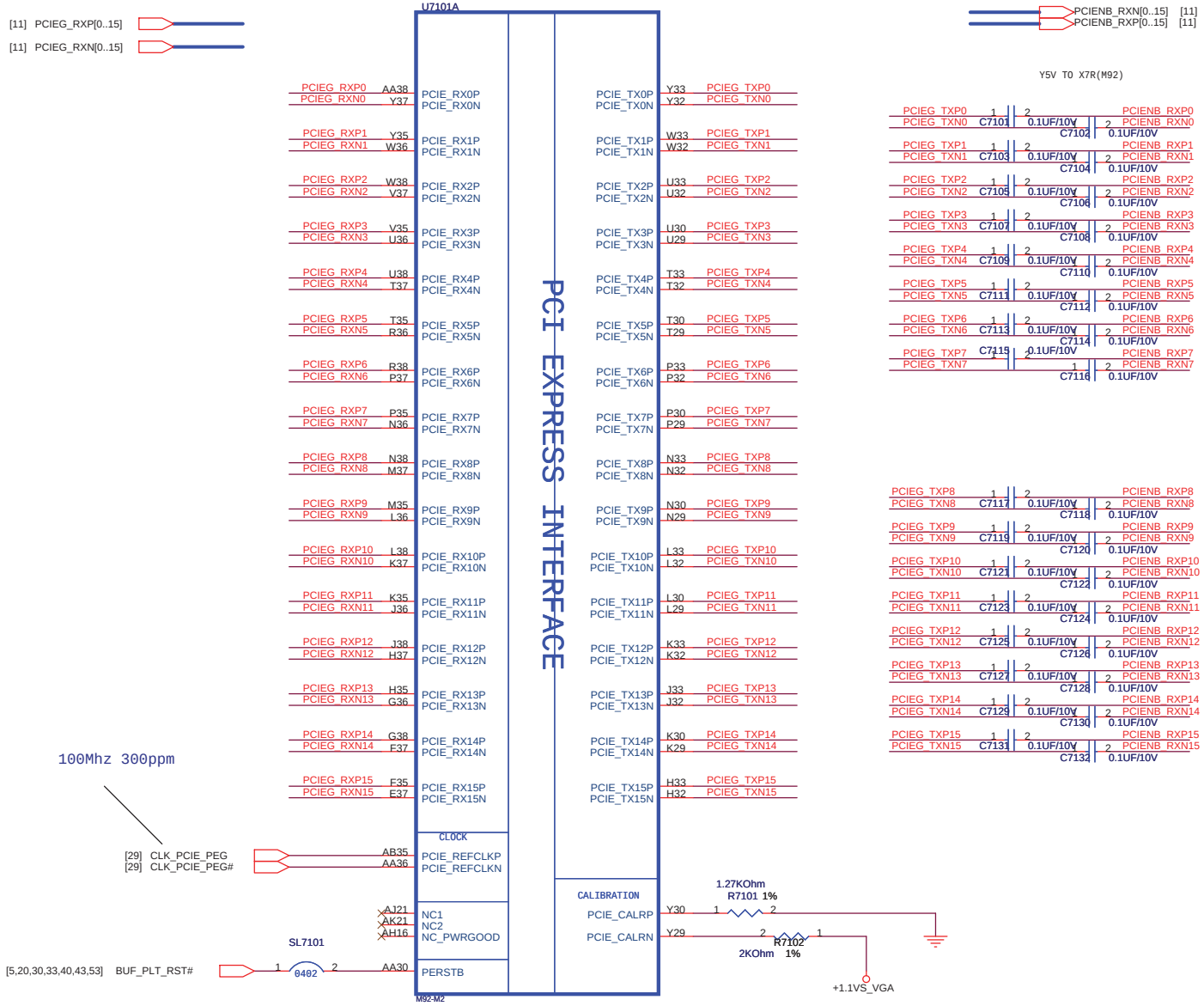
36. Add C4019 for EMI 090525

37. Change SL4610,SL4610 to 0ohm 090526

ASUSTeK COMPUTER INC. NB1		Title : HISTORY	
		Engineer: <OrgAddr1>	
Size: Custom	Project Name: F5Z		Rev: 2.05
Date: Friday, May 29, 2009		Sheet 69 of 91	

ASUS	Title : <Title>	
<OrgName>	Engineer: <OrgAddr1>	
Size: A	Project Name: <Doc>	Rev: <RevCode>
Date: Tuesday, May 26, 2009	Sheet 70 of 91	

notice the net name.RX&TX



<Variant Name>

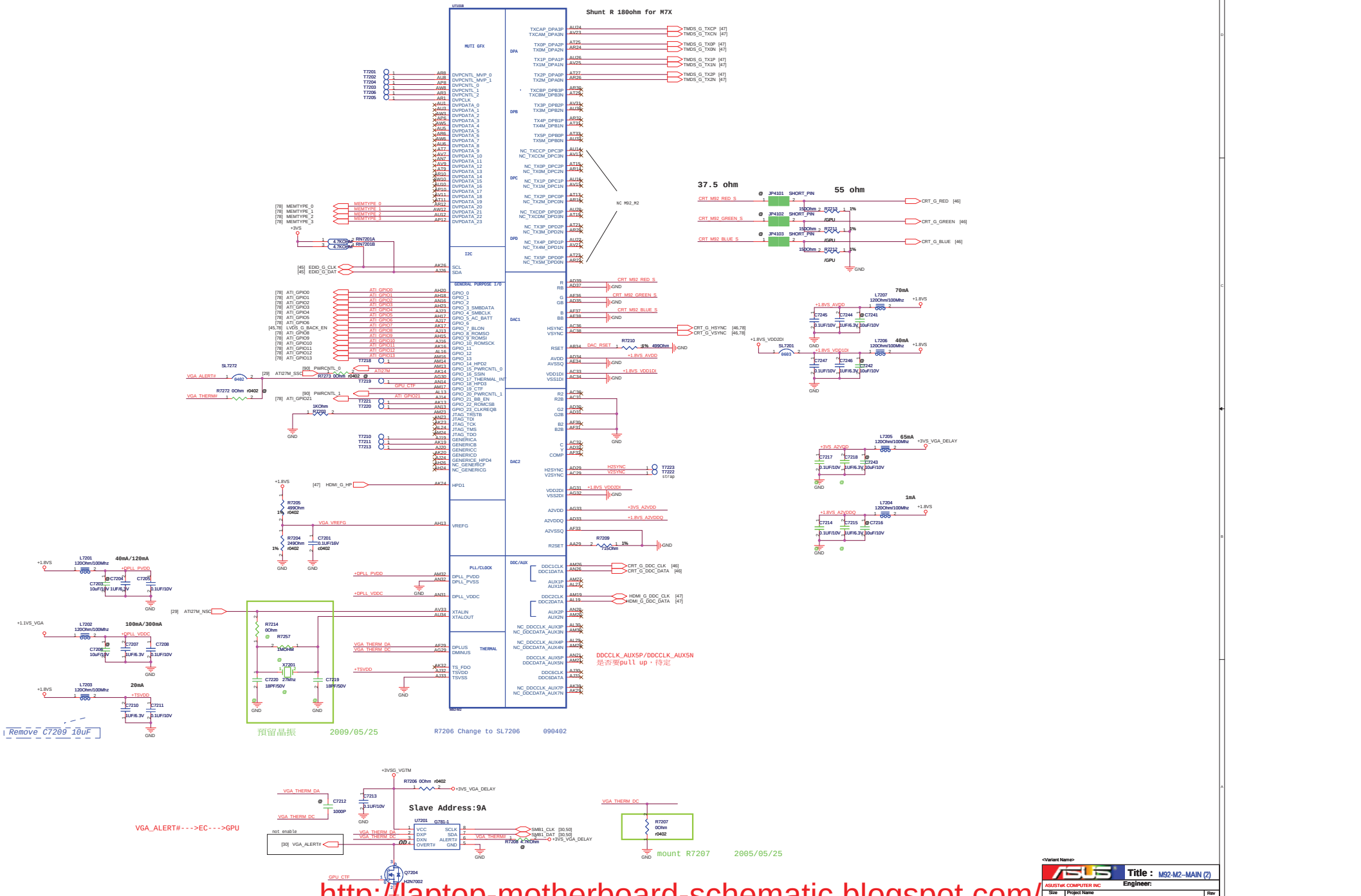
ASUSTeK COMPUTER INC

Title : M92-M2--PCIE (1)

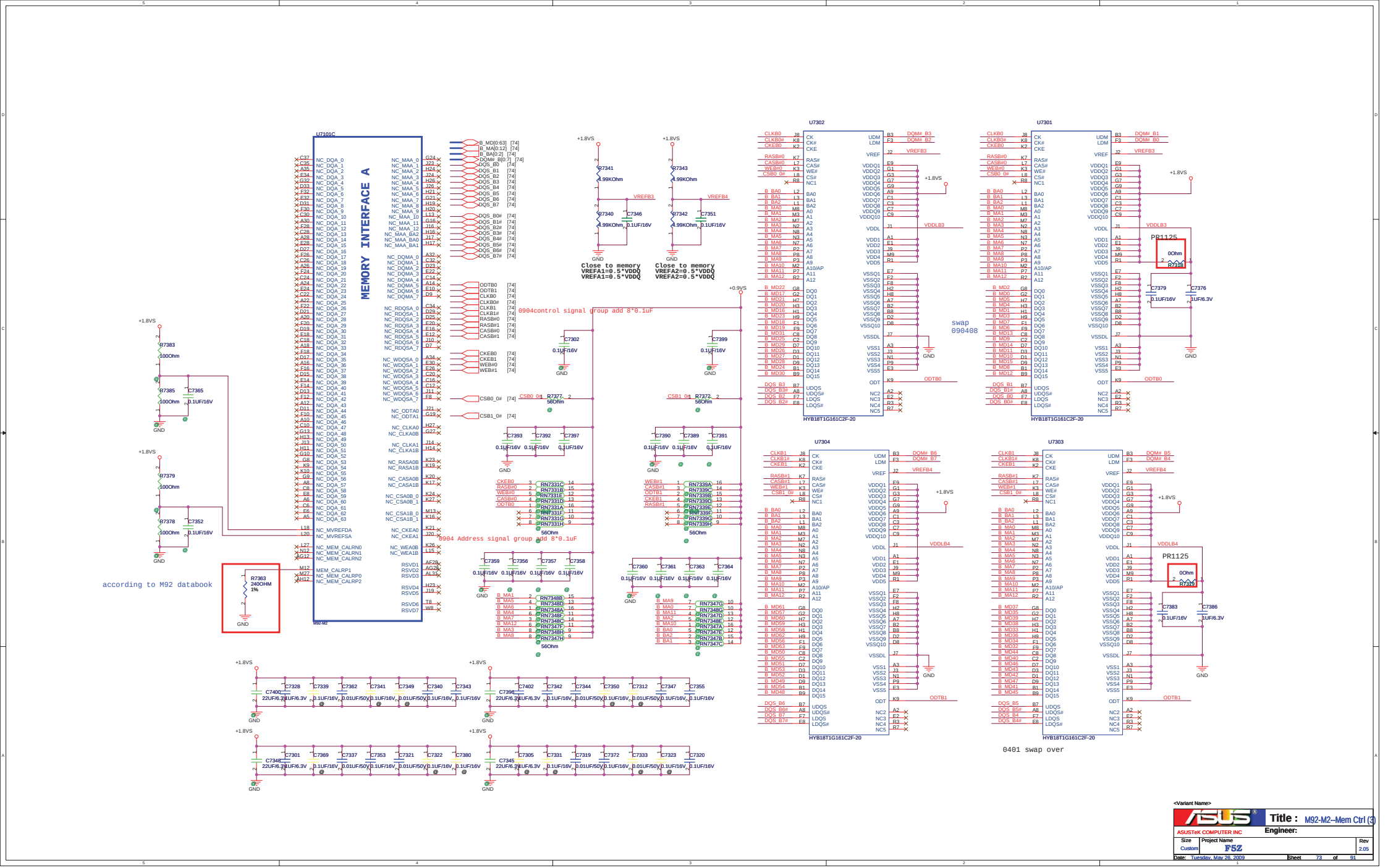
Engineer:

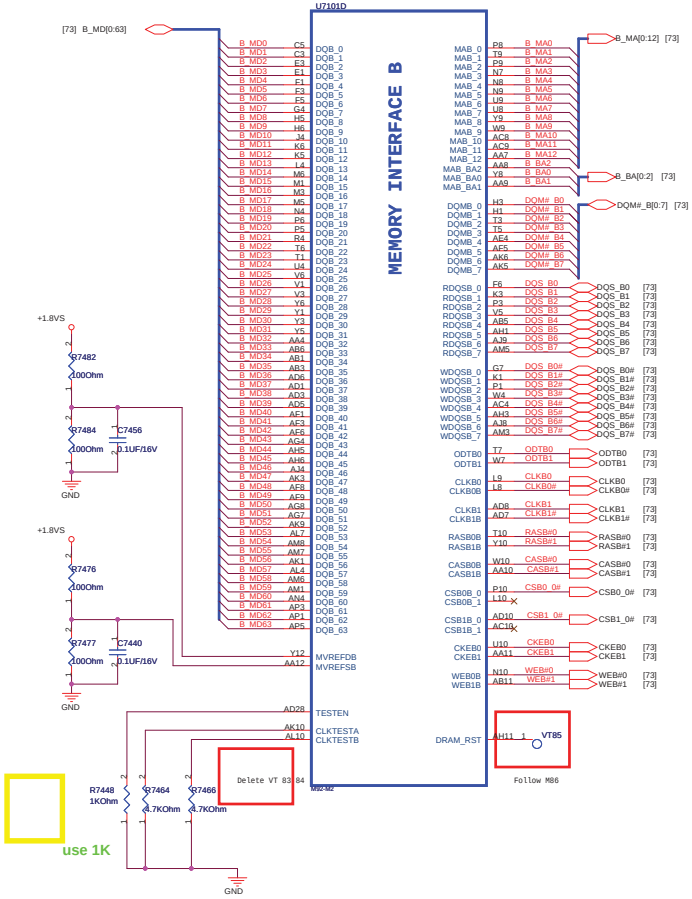
Size	Project Name	Rev
Custom	F5Z	2.05

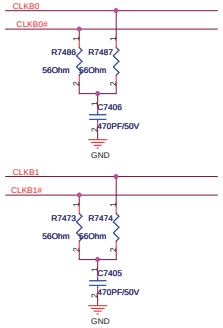
Date: Tuesday, May 26, 2009 Sheet 71 of 91



Title :	M92-M2--MAIN (2)
Engineer:	
ASUSTeK COMPUTER INC	
Size: Custom	Project Name: F52
Rev: 2.05	
Date: Friday, May 29, 2009	Sheet 72 of 91







Del 4 Vram
090323

<Variant Name>

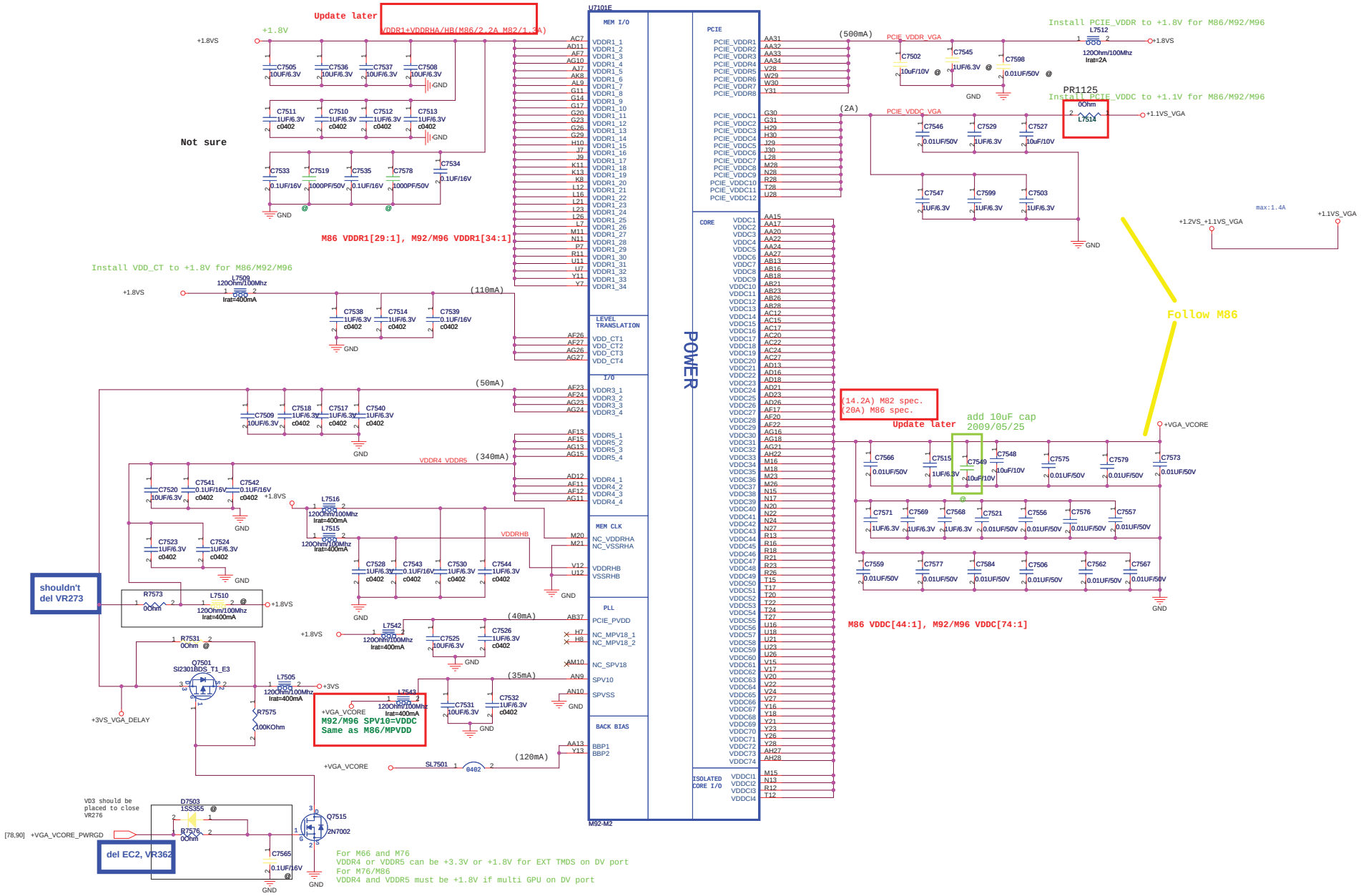
Title : M92S2-MEM VRAM(4)

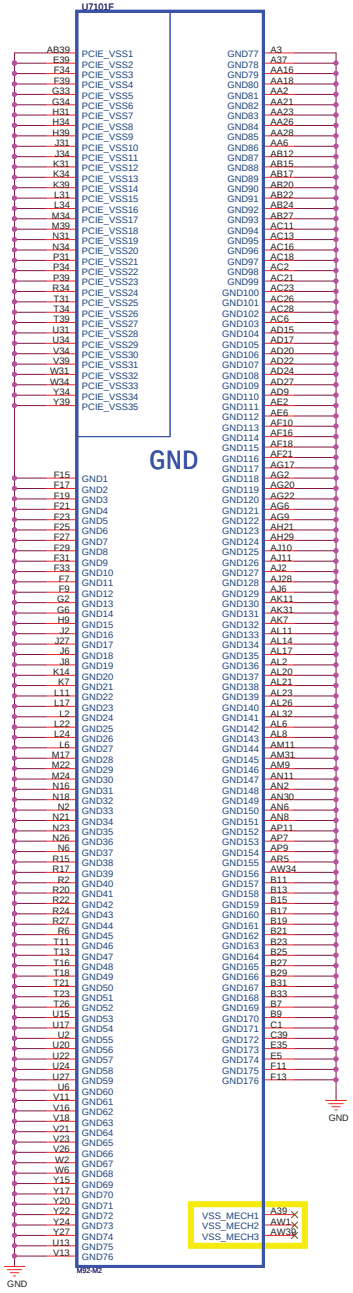
ASUSTeK COMPUTER INC

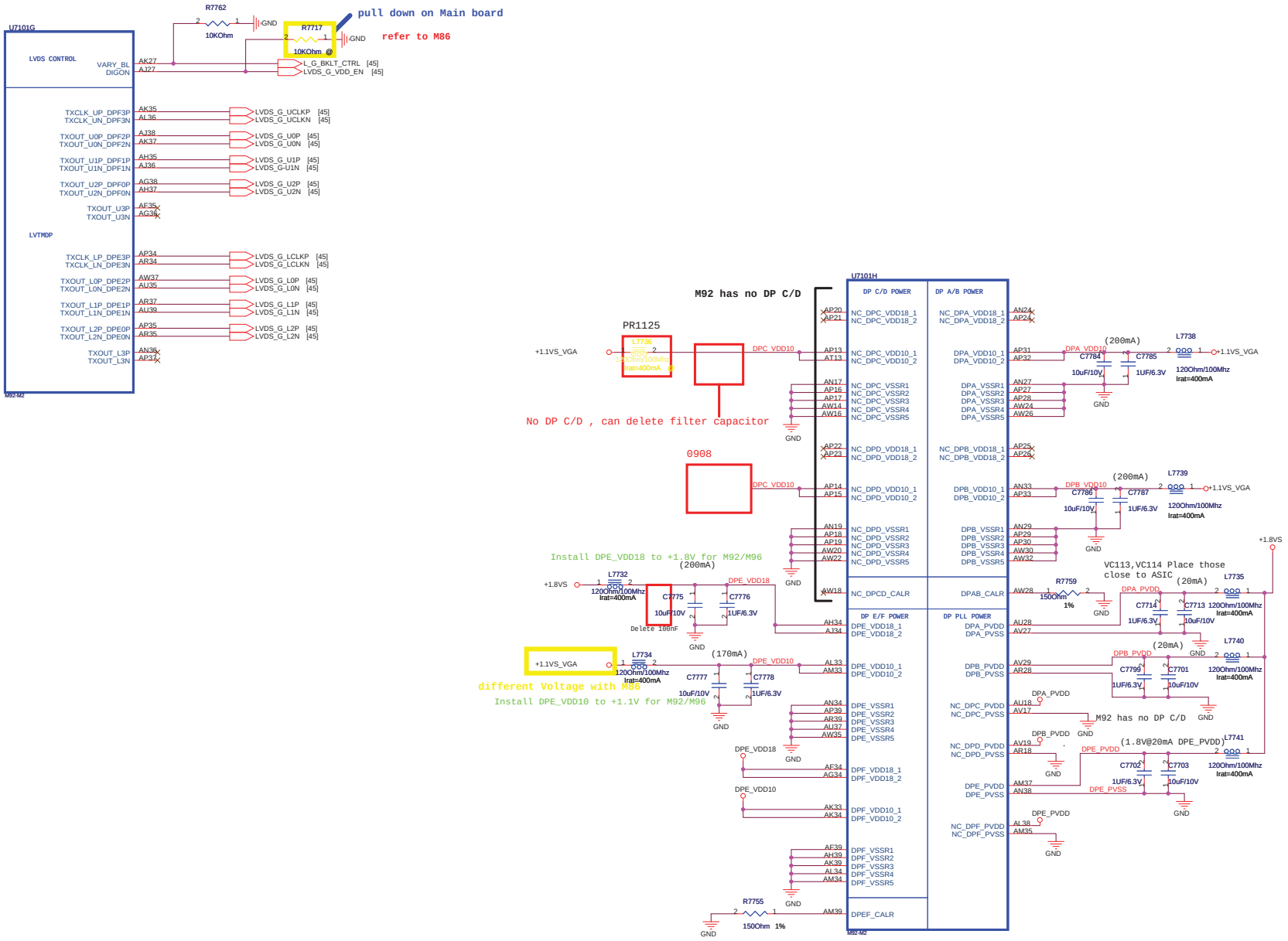
Engineer:

Size	Project Name	Rev
Custom	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 74 of 91







<Variant Name>

ASUSTeK COMPUTER INC.

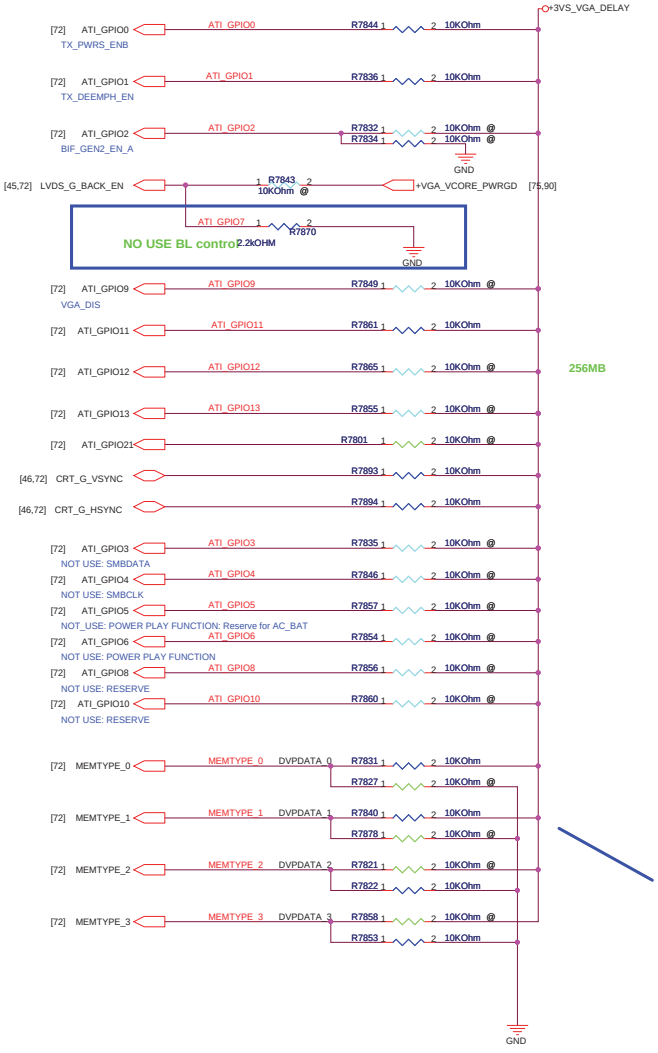
Title : M92S2-LVDS (6)

Engineer:

Size	Project Name	Rev
C	F5Z	2.05

Date: Tuesday, May 26, 2009 Sheet 77 of 91

OPTION STRAPS



M92 Straps

	STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
	VIP_DEVICE_STRAP_EN	V2SYNC	0 - Ignore VIP device straps (DVPDATA_20) 1 - Use VIP device straps (DVPDATA_20)	0 (internal pull-down)
OK	TX_PWRS_ENB	GPIO0	Tansmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing This setting can only be used if the PCIE bus design meets the "Low Loss interconnect" requirements.	0 (internal pull-down)
OK	TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled MXM and add-in boards	0 (internal pull-down)
OK	BIF_GEN2_EN_A	GPIO2	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
OK	VGA_DIS	GPIO9	0 - VGA Controller capacity enabled 1 - The device will not be recognized as the system's VGA controller	0 (internal pull-down)
OK	ROMIDCFG(2:0)	GPIO(13:11)	If BIOS_ROM_EN=1,then Config[2:0]defines the ROM type. If BIOS_ROM_EN=0,then Config[2:0]deifnes the primary memoru apeture size. 128MB---x000 32MB---Not Support 2GB---Not Support 256MB---x001 512MB--Not Support 4GB---Not Support 64MB---x010 1GB------Not Support	0000 (internal pull-down)
OK	BIOS_ROM_EN	GPIO22_ROMCSB	Enable external BIOS ROM device 0-Disable external BIOS ROM device 1-Enable external BIOS ROM device	0 (internal pull-down)
OK OK	AUD[1] AUD[0]	PEG_CRT_HSYNC_VGA PEG_CRT_VSYNC_VGA	AUD[1:0]: 00: No audio function; 01: Audio for DisplayPort and HDMI if adapter is detected; 10: Audio for DisplayPort only; 11: Audio for both DisplayPort and HDMI.	0 (internal pull-down)
OK OK	Reserved	H2SYNC GPIO_21_BB_EN GENERICC	ATI internal use only . THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET.	0 (internal pull-down)
	AUDIO_EN	VIP_3	Enable HD Audio function in the PCI configuration space 0 - Disable HD Audio 1 - Enable HD Audio	0 (internal pull-down)
	64BAR_EN_A	VIP_5	Enable 64-bit BARs Most commonly this strap is left at the default (32-bit BARs)	0 (internal pull-down)
	MSI_DIS	VIP_1	Disable Message Signaled Interrupt is both a ROM strap and a pin strap. The pin strap is only applicable if a BIOS ROM is not present	0 (internal pull-down)
	VIP_DEVICE	VHAD_0	VIP_DEVICE_STRAP_EN is set 0 =>not used VIP Host interface VIP_DEVICE_STRAP_EN is set 1 =>used VIP Host interface	0 (internal pull-down)
	DEBUG ACCESS	GPIO4	Debug_access strap 3.3V ---ON 0V------OFF	0 (internal pull-down)
	DEBUG_I2C_ENABLE	GPIO6	ATI internal use only . Other logic must not affect this signal during RESET Reconnended to 0	0 (internal pull-down)

0010-DDR2 Qimonda(64MX16) 512MB
Mount: VR27, VR40, VR22, VR353
Unmount: VR31, VR41, VR21, VR352

0011-DDR2 Qimonda(64MX16) 1G
Mount: VR31, VR40, VR22, VR353
Unmount: VR27, VR41, VR21, VR352

0100-DDR2 Samsung(64MX16) 512MB
Mount: VR27, VR41, VR21, VR353
Unmount: VR31, VR40, VR22, VR352

0101-DDR2 Samsung(64MX16) 1G
Mount: VR31, VR41, VR21, VR353
Unmount: VR27, VR40, VR22, VR352

Memory ID Board Straps

Vendor	DVPDATA(23,22,21,20)	ID	DDR2 Memory Type	Channel Size
Qimonda	0000	0	32M*16 (256M)	B channel
	0001	1	32M*16 (512M)	B channel dual-link
	0010	2	64M*16 (512M)	B channel
	0011 M92-M2	3	64M*16 (1G)	B channel dual-link
Samsung	0100	4	64M*16 (512MB)	B channel
	0101 M92-M2	5	64M*16 (1G)	B channel dual-link
	0110	6	32M*16 (256MB)	B channel
	0111	7	32M*16 (512MB)	B channel dual-link
Hynix	1000	8	32M*16 (256M)	B channel
	1001	9	32M*16 (512M)	B channel dual-link
	1010	10	64M*16 (512M)	B channel
	1011 M92-M2	11	64M*16 (1G)	B channel dual-link
	1100	12	TBD	
	1101	13		
	1110	14		
Micron	1111	15	64M*16 (1G)	B channel dual-link

M92-M2 only support B channel

<Variant Name>

ASUSTeK COMPUTER INC.

Title : *

Engineer:

Size	Project Name	Rev
C	F5Z	2.05

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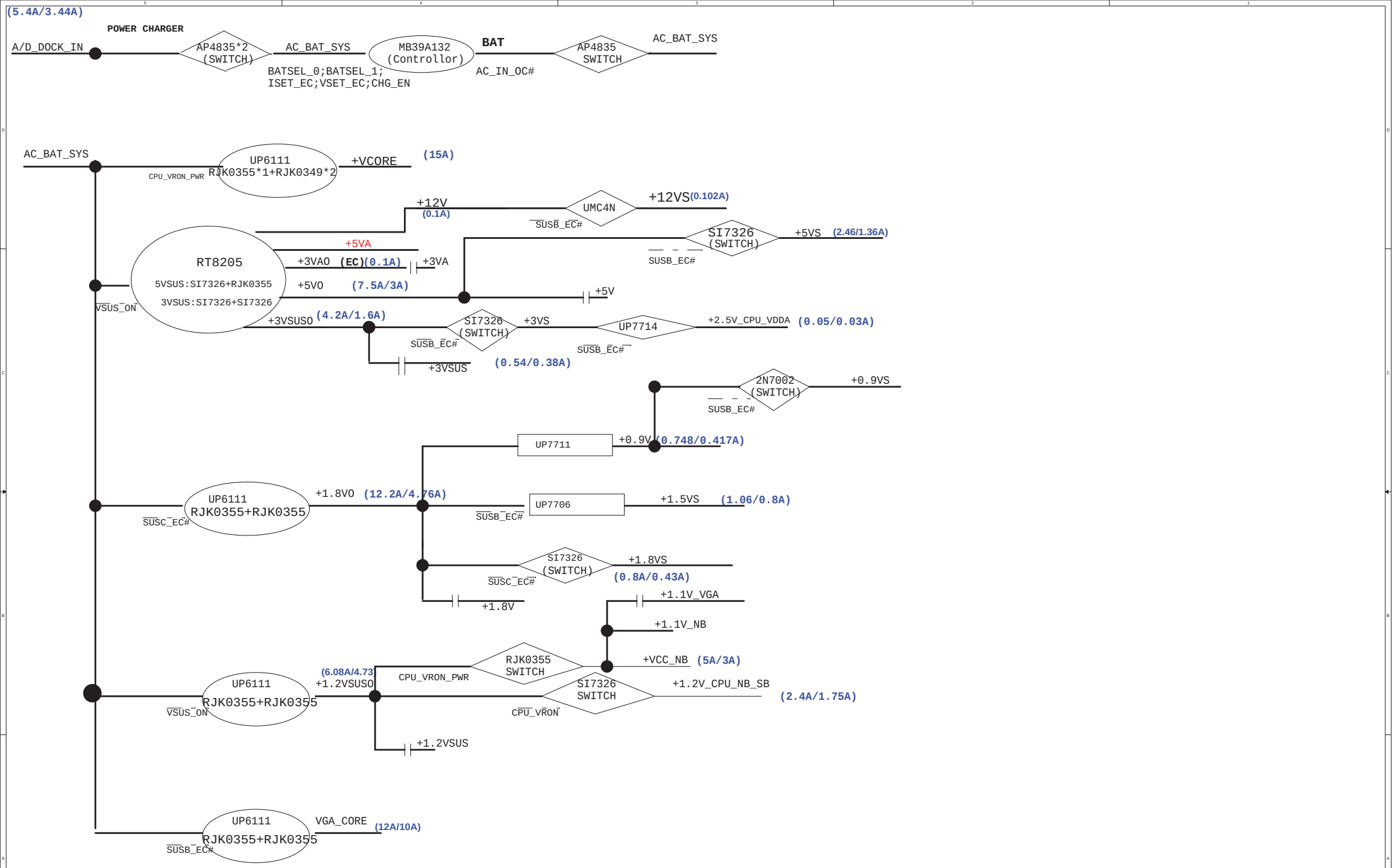
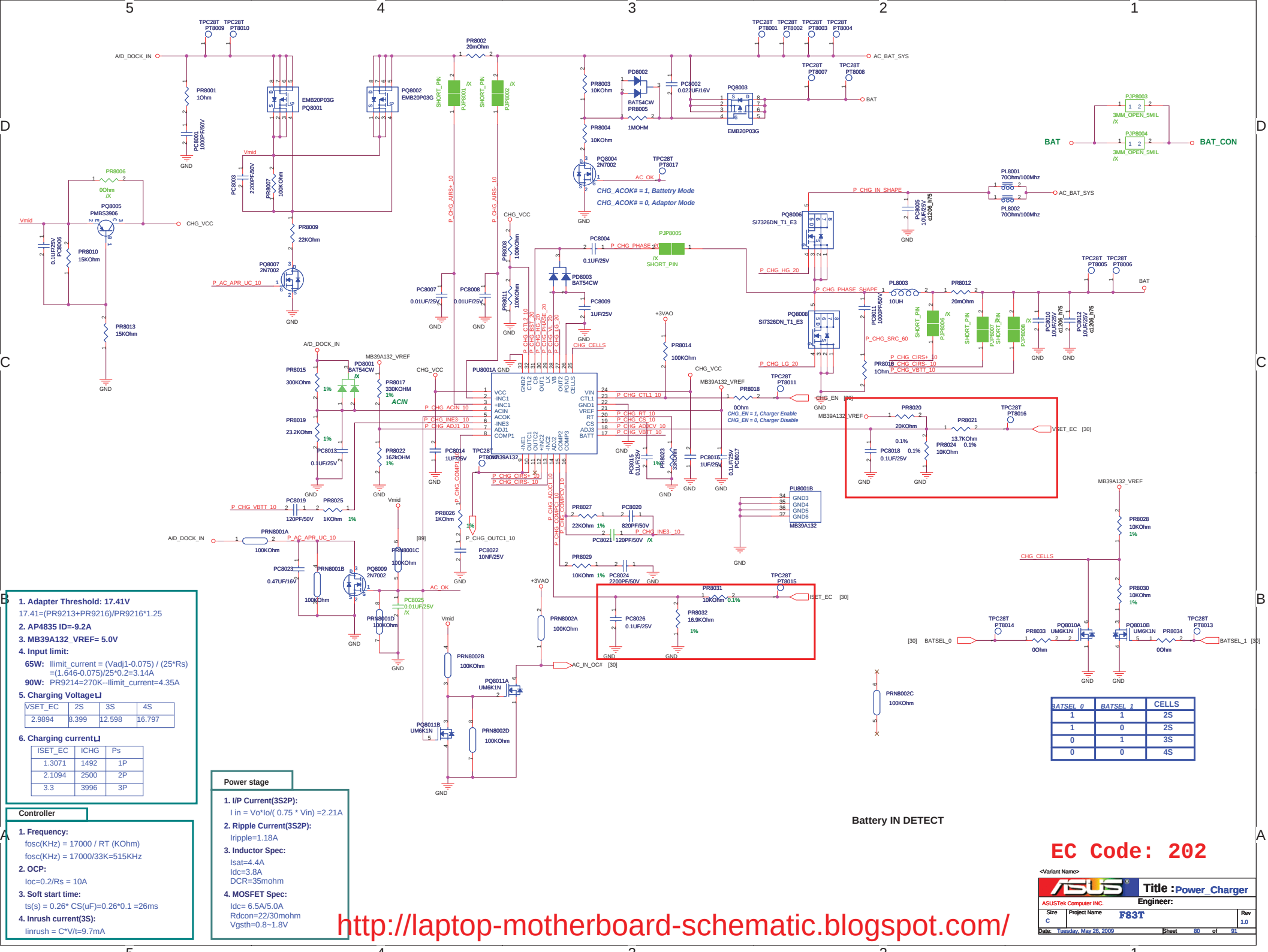
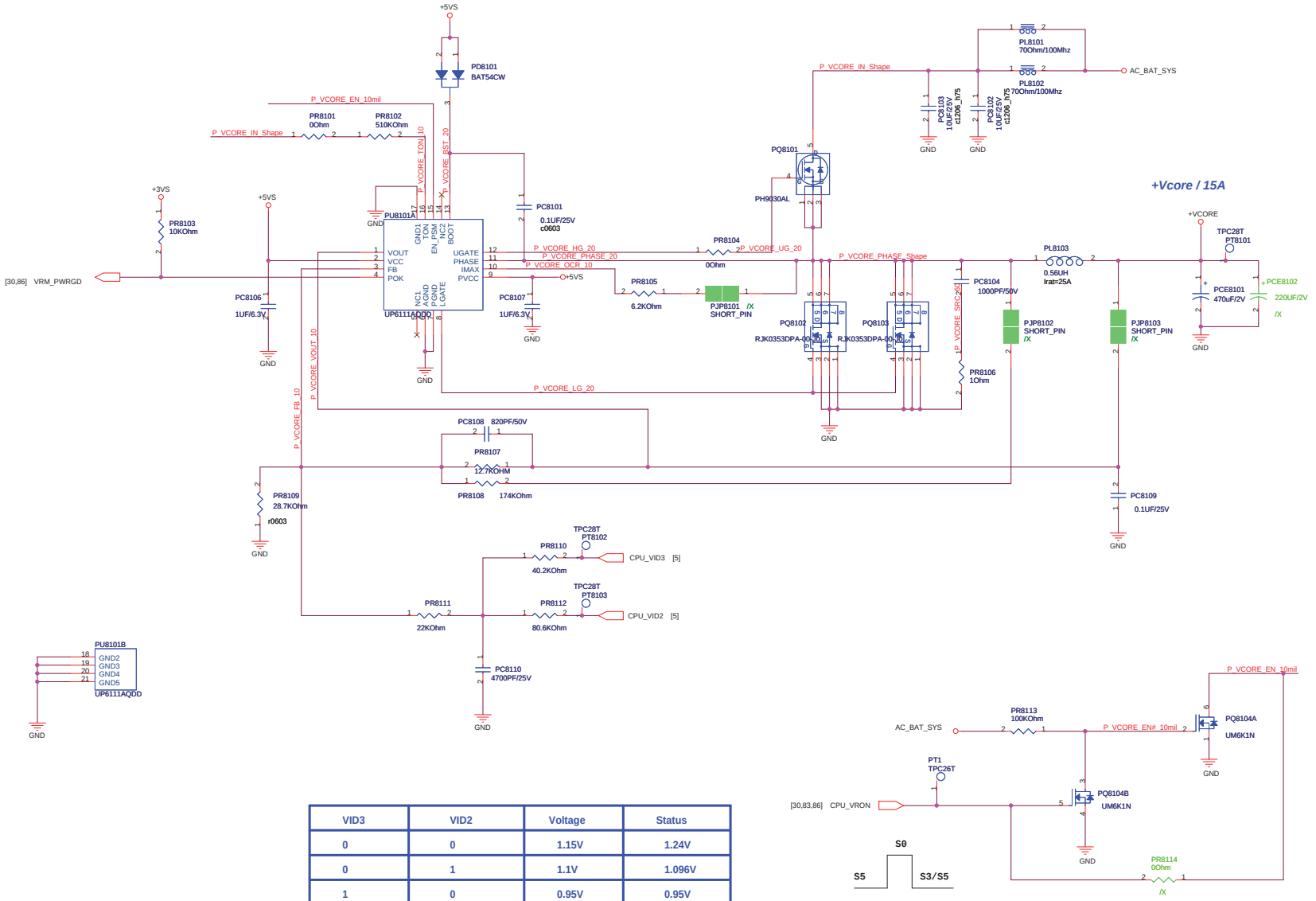



A/D_DOCK_IN
AC_BAT_SYS
BAT
BAT_CON
CHG_VCC
Vmid
+3VAO
MB39A132_VREF
P_CHG_ACIN_10
P_CHG_INE3-_10
P_CHG_ADJ1_10
P_CHG_VBTT_10
P_CHG_CIRS+_10
P_CHG_CIRS-_10
P_CHG_COMP1_10
P_CHG_OUTC1_10
P_CHG_ADJC1_10
P_CHG_COMPC1_10
P_AC_APR_UC_10
P_CHG_AIRS+_10
P_CHG_AIRS-_10
P_CHG_PHASE_20
P_CHG_HG_20
P_CHG_LG_20
P_CHG_CTL1_10
P_CHG_CTL2_10
P_CHG_BST_20
P_CHG_VC_20
P_CHG_IN_SHAPE
P_CHG_PHASE_SHAPE
P_CHG_SRC_60
CHG_EN [30]
AC_OK
AC_IN_OC# [30]
ISET_EC [30]
VSET_EC [30]
BATSEL_0 [30]
BATSEL_1 [30]
CHG_CELLS
PR8001 1Ohm
PC8001 1000PF/50V
EMB20P03G PQ8001
PQ8002 EMB20P03G
PR8002 20mOhm
PJP8001 /X
PJP8002 /X
PR8003 10KOhm
PD8002 BAT54CW PR8005
PC8002 0.022UF/16V
PQ8003 EMB20P03G
PR8004 10KOhm
1MOHM
PQ8004 2N7002
TPC28T PT8017
CHG_ACOK# = 1, Battetry Mode
CHG_ACOK# = 0, Adaptor Mode
PJP8003 3MM_OPEN_5MIL /X
PJP8004 3MM_OPEN_5MIL /X
PL8001 70Ohm/100Mhz
PL8002 70Ohm/100Mhz
PC8005 1000PF/50V c1206_h75
PQ8006 SI7326DN_T1_E3
PJP8005 /X SHORT_PIN
PC8004 0.1UF/25V
PR8006 0Ohm /X
PQ8005 PMBS3906
PC8006 0.1UF/25V
PR8010 15KOhm
PR8013 15KOhm
PR8009 22KOhm
PQ8007 2N7002
PC8003 2200PF/50V
PR8007 100K Ohm
PR8008 100KOhm
PC8007 0.01UF/25V
PC8008 0.01UF/25V
PR8011 100KOhm
PD8003 BAT54CW
PC8009 1UF/25V
CHG_CELLS
PU8001A
PR8014 100KOhm
PQ8008 SI7326DN_T1_E3
PL8003 10UH
PR8012 20mOhm
PC8011 1000PF/50V
PC8010 10UF/25V c1206_h75
PC8012 10UF/25V c1206_h75
PJP8006 /X
PJP8007 /X
PJP8008 /X
PR8015 300KOhm 1%
PD8001 BAT54CW /X
PR8017 330KOHM 1%
ACIN
PR8019 23.2KOhm 1%
PC8013 0.1UF/25V
PR8022 162kOHM 1%
PC8014 1UF/25V
PC8015 0.1UF/25V
PR8023 33KOhm 1%
PC8016 1UF/25V
PC8017 0.1UF/25V
PR8018 0Ohm
CHG_EN = 1, Charger Enable
CHG_EN = 0, Charger Disable
PR8020 20KOhm 0.1%
PR8021 13.7KOhm 0.1%
PR8024 10KOhm 0.1%
PC8018 0.1UF/25V
PC8019 120PF/50V
PR8025 1KOhm 1%
PR8026 1KOhm 1%
PC8022 10NF/25V
PRN8001A 100KOhm
PC8023 0.47UF/16V
PRN8001B 100KOhm
PQ8009 2N7002
PC8025 0.01UF/25V /X
PRN8001C 100KOhm
PRN8001D 100KOhm
PR8027 22KOhm 1%
PC8020 820PF/50V
PC8021 120PF/50V /X
PR8029 10KOhm 1%
PC8024 2200PF/50V
PR8031 10KOhm 0.1%
PR8032 16.9KOhm 1%
PC8026 0.1UF/25V
PRN8002A 100KOhm
PRN8002B 100KOhm
PQ8011A UM6K1N
PQ8011B UM6K1N
PRN8002D 100KOhm
PRN8002C 100KOhm
PR8028 10KOhm 1%
PR8030 10KOhm 1%
PR8033 0Ohm
PR8034 0Ohm
PQ8010A UM6K1N
PQ8010B UM6K1N
TPC28T PT8014
TPC28T PT8013
BATSEL_0 | BATSEL_1 | CELLS
1 | 1 | 2S
1 | 0 | 2S
0 | 1 | 3S
0 | 0 | 4S
1. Adapter Threshold: 17.41V
17.41=(PR9213+PR9216)/PR9216*1.25
2. AP4835 ID=-9.2A
3. MB39A132_VREF= 5.0V
4. Input limit:
65W: Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.646-0.075)/25*0.2=3.14A
90W: PR9214=270K--Ilimit_current=4.35A
5. Charging Voltage
VSET_EC | 2S | 3S | 4S
2.9894 | 8.399 | 12.598 | 16.797
6. Charging current
ISET_EC | ICHG | Ps
1.3071 | 1492 | 1P
2.1094 | 2500 | 2P
3.3 | 3996 | 3P
Controller
1. Frequency:
fosc(KHz) = 17000 / RT (KOhm)
fosc(KHz) = 17000/33K=515KHz
2. OCP:
Ioc=0.2/Rs = 10A
3. Soft start time:
ts(s) = 0.26* CS(uF)=0.26*0.1 =26ms
4. Inrush current(3S):
Iinrush = C*V/t=9.7mA
Power stage
1. I/P Current(3S2P):
I in = Vo*Io/(0.75 * Vin) =2.21A
2. Ripple Current(3S2P):
Iripple=1.18A
3. Inductor Spec:
Isat=4.4A
Idc=3.8A
DCR=35mohm
4. MOSFET Spec:
Idc= 6.5A/5.0A
Rdcon=22/30mohm
Vgsth=0.8~1.8V
Battery IN DETECT
EC Code: 202
<Variant Name>
Title : Power_Charger
ASUSTek Computer INC.
Engineer:
Size C
Project Name F83T
Rev 1.0
Date: Tuesday, May 26, 2009
Sheet 80 of 91
http://laptop-motherboard-schematic.blogspot.com/



VID3	VID2	Voltage	Status
0	0	1.15V	1.24V
0	1	1.1V	1.096V
1	0	0.95V	0.95V
1	1	0.8V	0.805V

Controller

1. Voltage & Current:
   VCORE: 15A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   SetPR8105=12K
   Iocp=Rocp*20/Rds(on)=12*20/7.6=31.6A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =470UF
   I inrush=0.38A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.75 * Vin) =1.16A
2. Ripple Current:
   Iripple=3.5A
3. Dynamic:
   Ipeak=15A
   ESR=9mohm
   V=122mV
4. Inductor Spec:
   Isat=40A
   Idc=25A
   DCR=1.6mohm
5. MOSFET Spec:
   L-side MOSFET:
   Rds(on)max=7.6mOhm
   (Vgs=4.5V)
   Icont=35A (T=25)
   Ipeak=140A (Pause<10us)

<Variant Name>

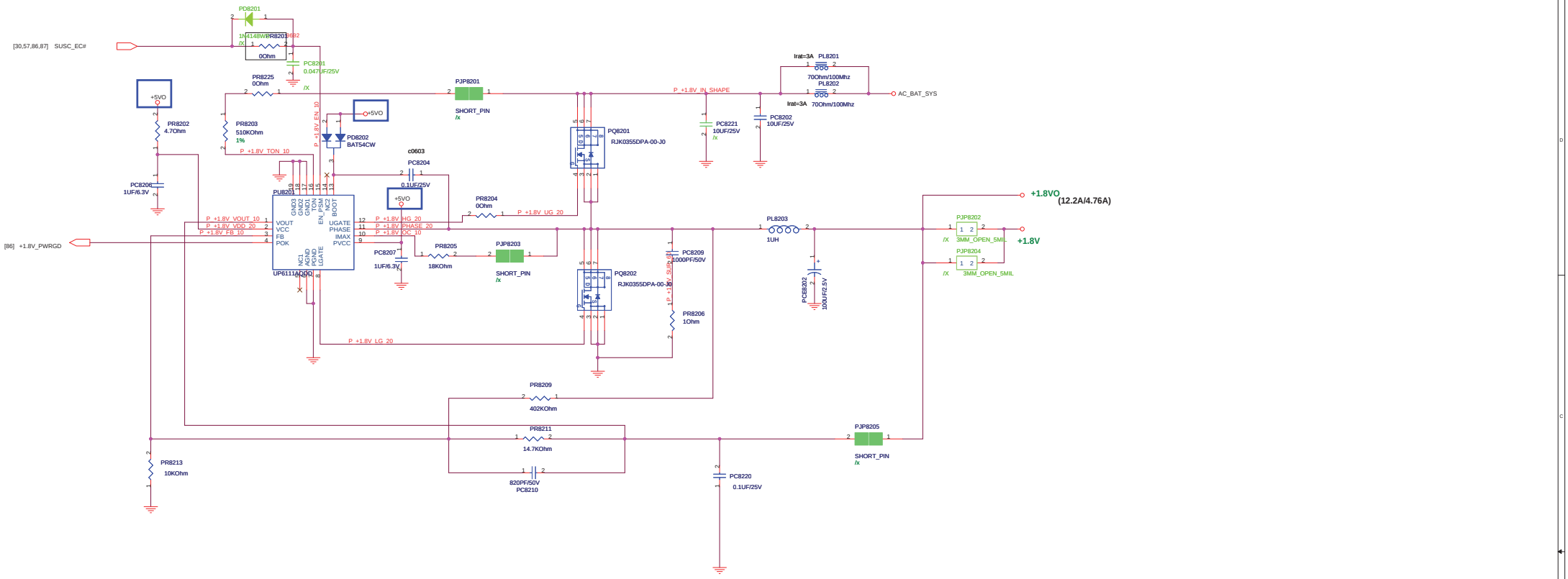
ASUSTeK COMPUTER INC

Title : Power_VCORE

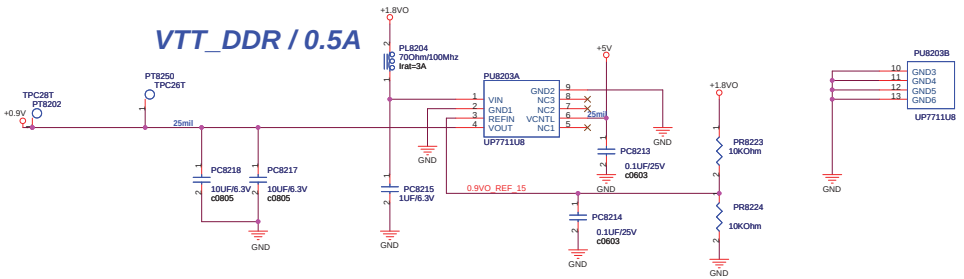
Engineer:

Size	Project Name	Rev
C	F83T	1.0

Date: Tuesday, May 26, 2009 Sheet 81 of 91



VTT_DDR / 0.5A



Controller

1. Voltage & Current:
   +1.8V:+1.8V&8A
2. Frequency:
   Ton=3.85p*Rt(on)/Vin-05=0.3us
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18kohm
   Iocp=Rocp*20/Rds(on)
   =20*18/16.5=21.8A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =100uF
   I
   inrush=0.133A

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.947A
2. Ripple Current:
   Iripple=2.342A
3. Ripple Voltage:
   Ipeak=(vin-vo)*D/(L*Fsw)=3.25A
   ESR=18mohm
   V=58.5mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+1.8V&+0.9V

Engineer:

Size	Project Name	Rev
A2		1.0

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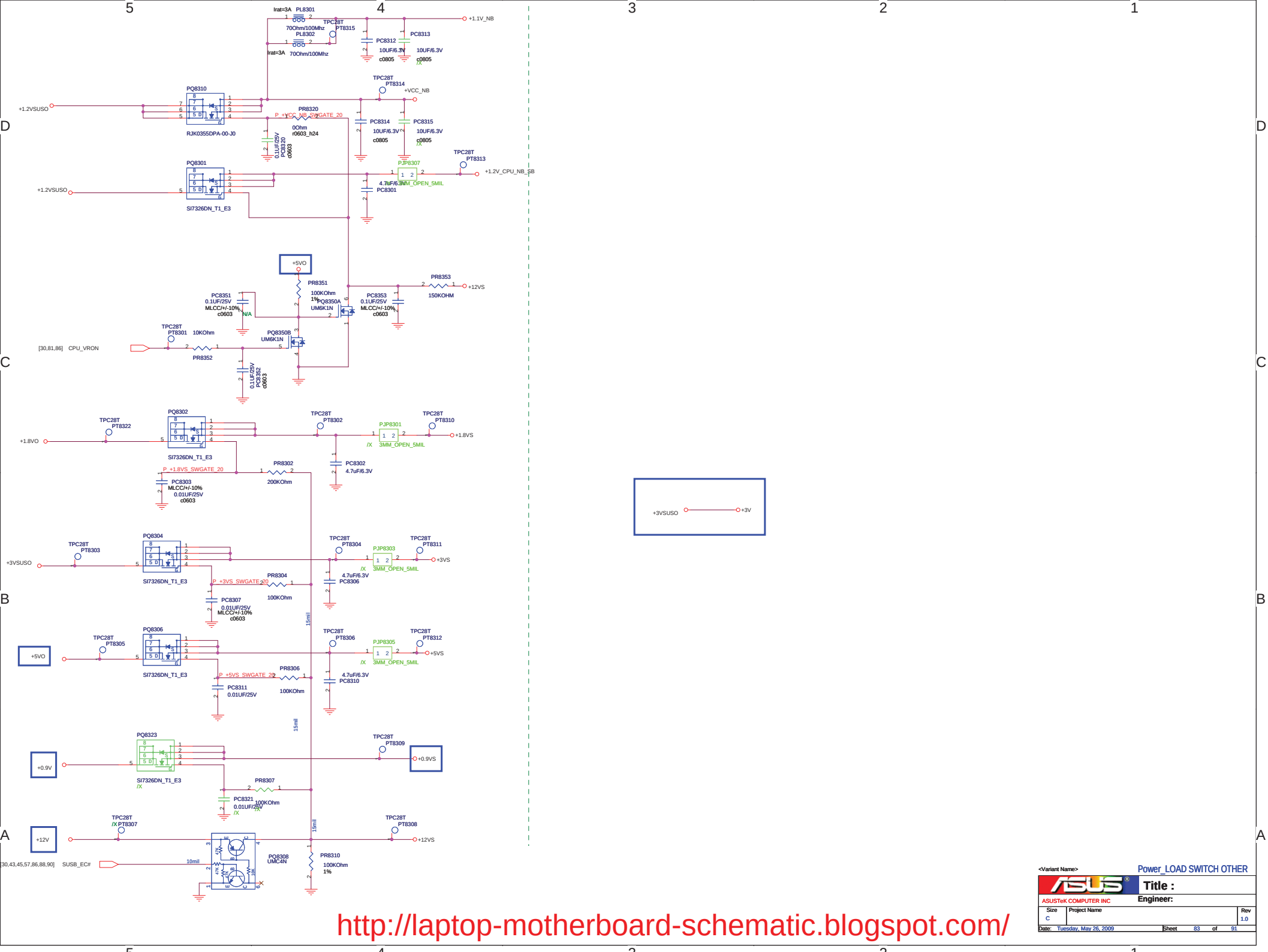


<variant_name>
Power_LOAD SWITCH OTHER

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
C		1.0

Date: Tuesday, May 26, 2009 Sheet 83 of 91
</variant_name>

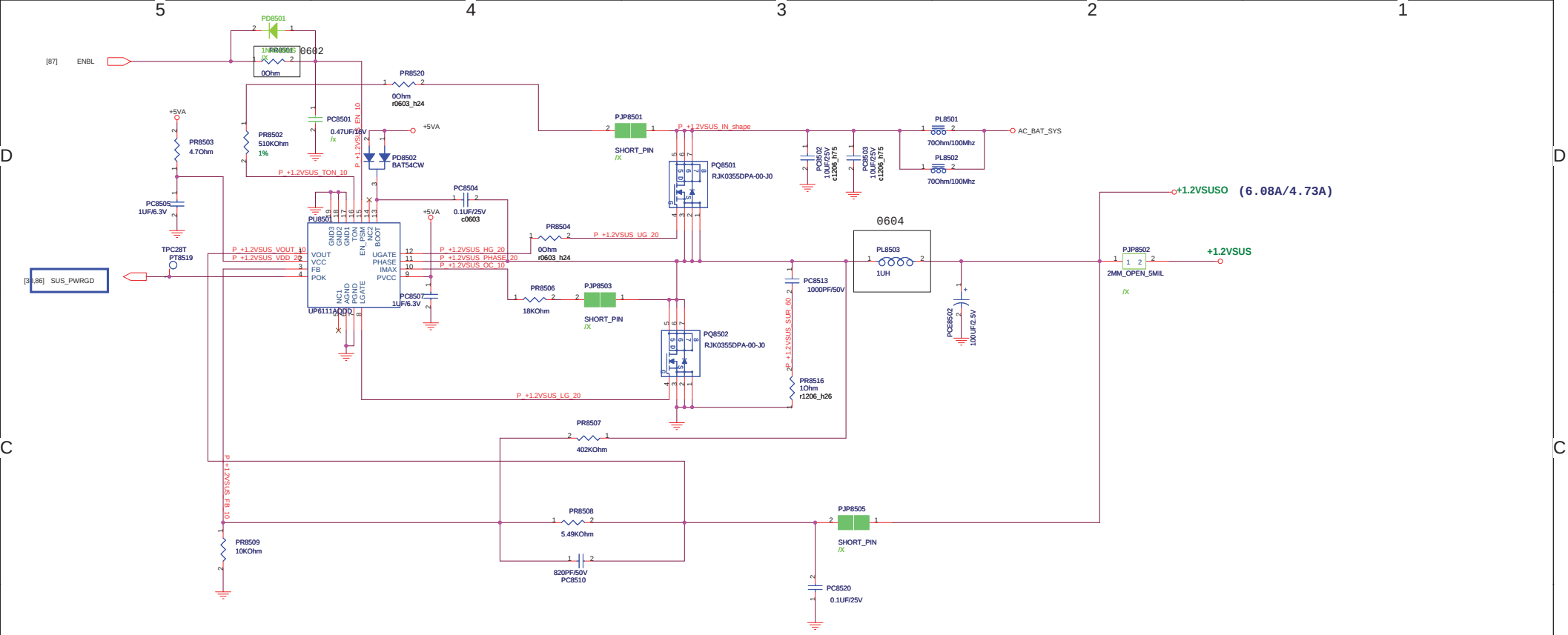
<Variant Name>

Title :

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
A		1.0
Date: Tuesday, May 26, 2009	Sheet 84 of 91	



Controller

1. Voltage & Current:
   +1.2VSUS:1.16V&12A
2. Frequency:
   Ton=3.85p*Rt(on)*Vo/Vin-05
   Frequency=Vout/(Vin*Ton)
   =500KHZ
3. OCP:
   Set PR7343=18Kohm
   Iocp=Rocp*20/Rds(on)=21.9A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =100uF
   I inrush=0.133A

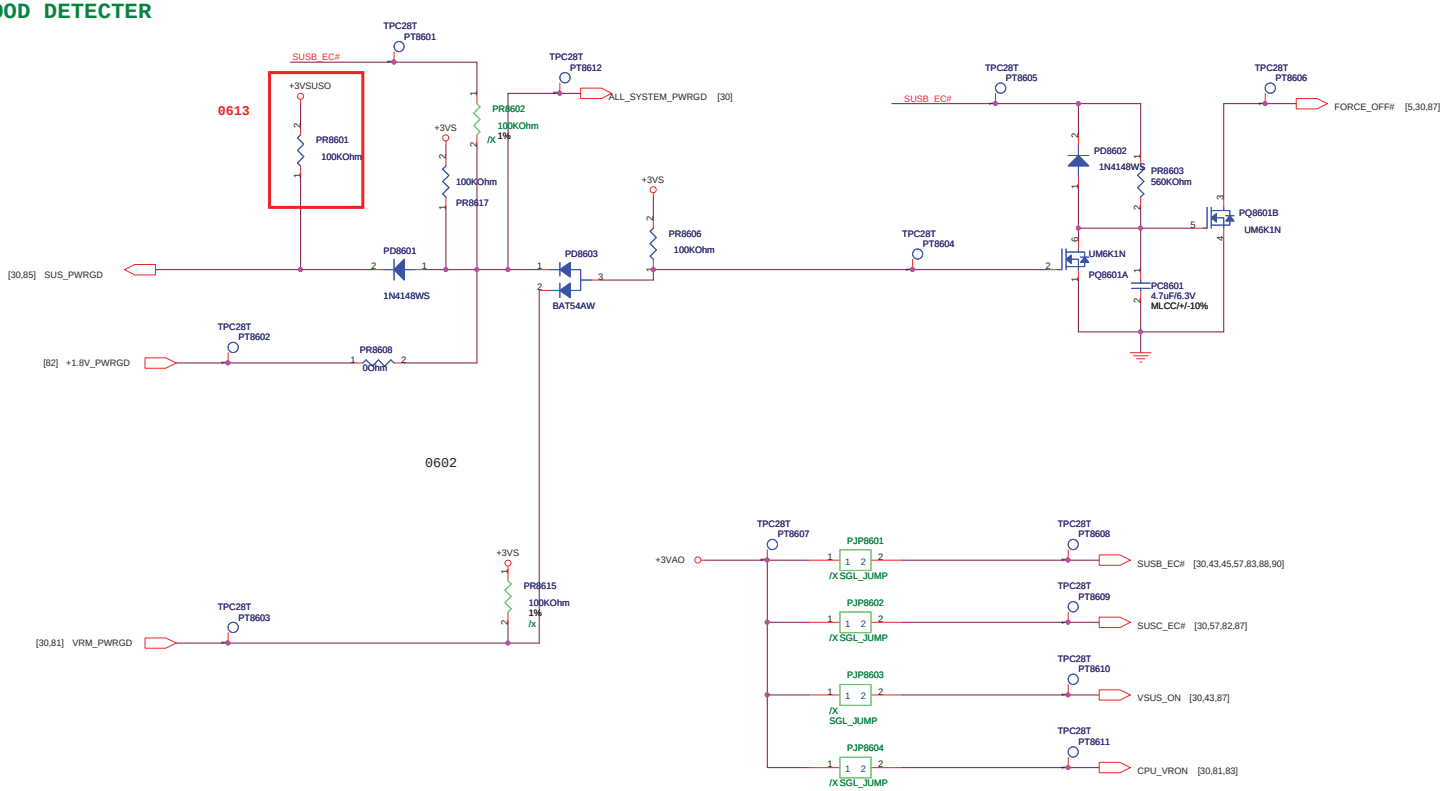
Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.915A
2. Ripple Current:
   Iripple=2.915A
3. Ripple Voltage:
   Ipeak=(Vin-Vo)*D/(L*Fsw)=2.24A
   ESR=18mohm
   V=40.32mV
4. Inductor Spec:
   Isat=22A
   Idc=11A
   DCR=9mohm
5. MOSFET Spec:
   H-side and L-side MOSFET:
   Rds(on)=16.5mOhm (Vgs=4.5V)
   Icont=30A (T=25)
   Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_1.2VSUS	
	Engineer:	
Size: C	Project Name	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 85 of 91	

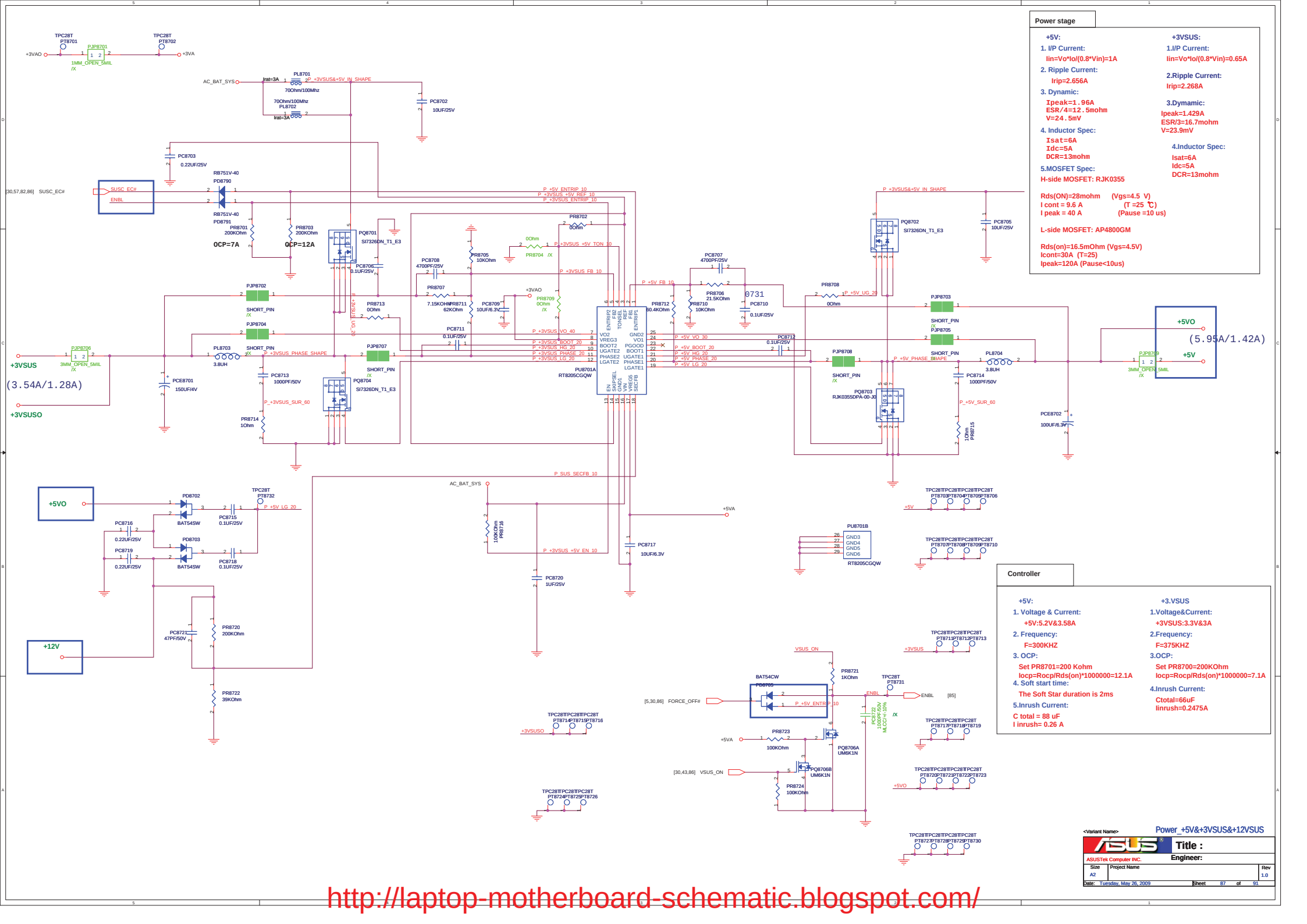
POWER GOOD DETECTER

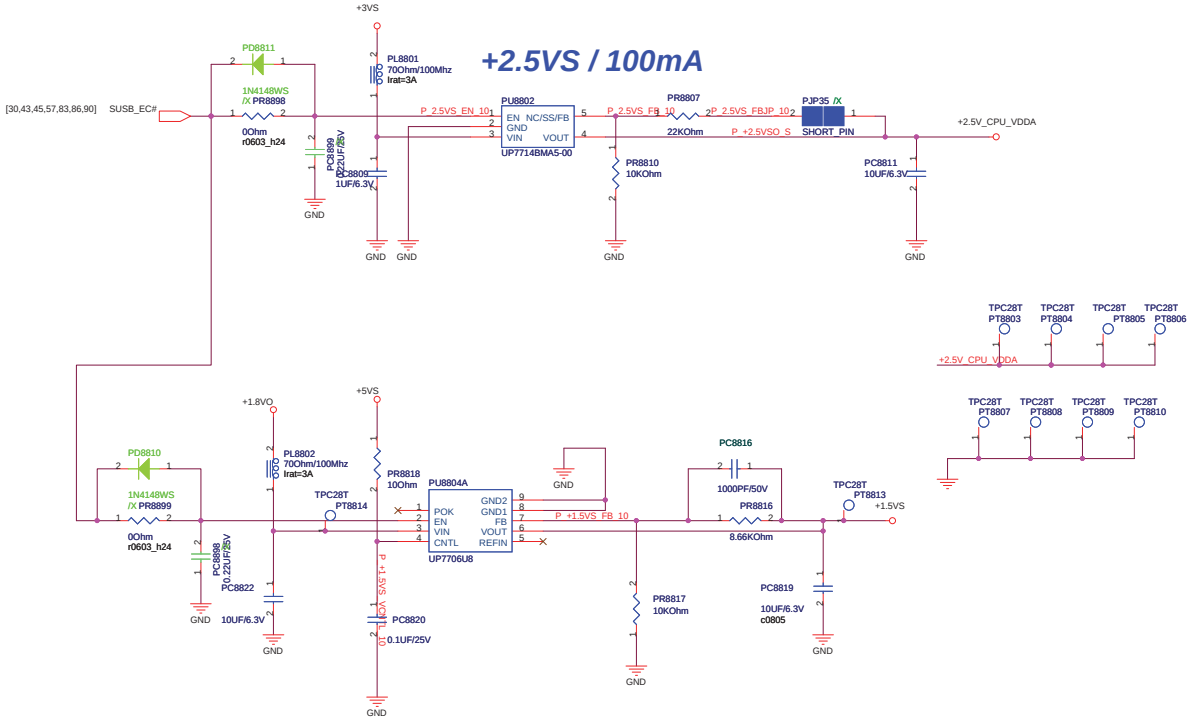


<Variant Name>

Power_GOOD_DETECTER

ASUSTeK COMPUTER INC	Title :	
	Engineer:	
Size: C	Project Name: F83T	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 86 of 91	





2.5V @ 0.1A

1. Dropout Voltage:

△V = 0.21V (Io =0.3A)

2. Current Limit:

I limit =320mA

3. Continue Current:

I cont =
300mA

4. Power Dissipation:

Rthjc = 250℃/W
Pd = 0.4W

5. EN Voltage:

V rising = 2V
V falling =
0.8V

6. Supply Voltage:

Vcc =3V

7. Inrush current:

T ss = 400us
C total =10uF
I inrush =
0.063A

<Variant Name>

Power +2.5V&+1.5VS&+1.1V NB

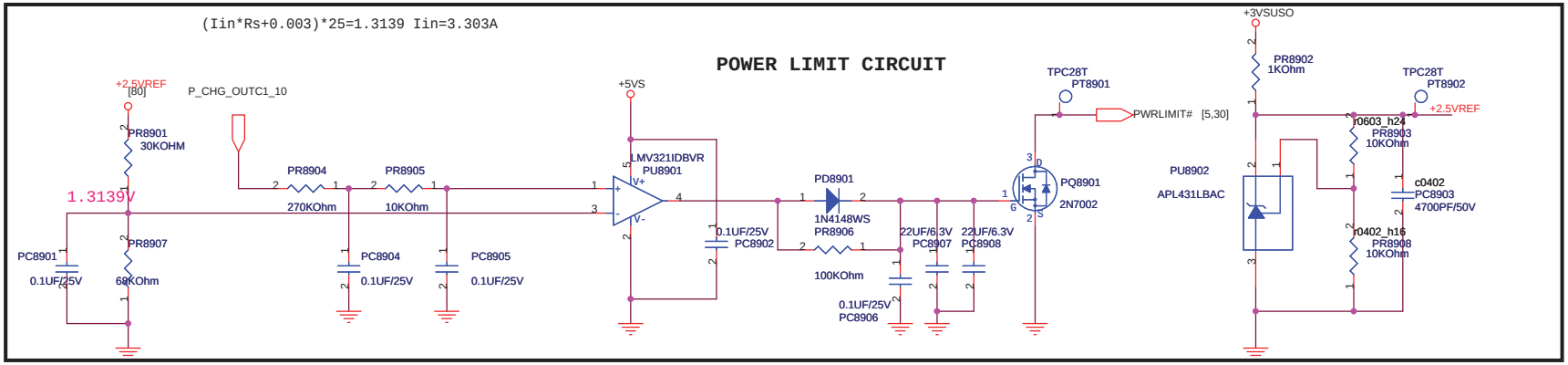
ASUSTek Computer INC.

Title :

Engineer:

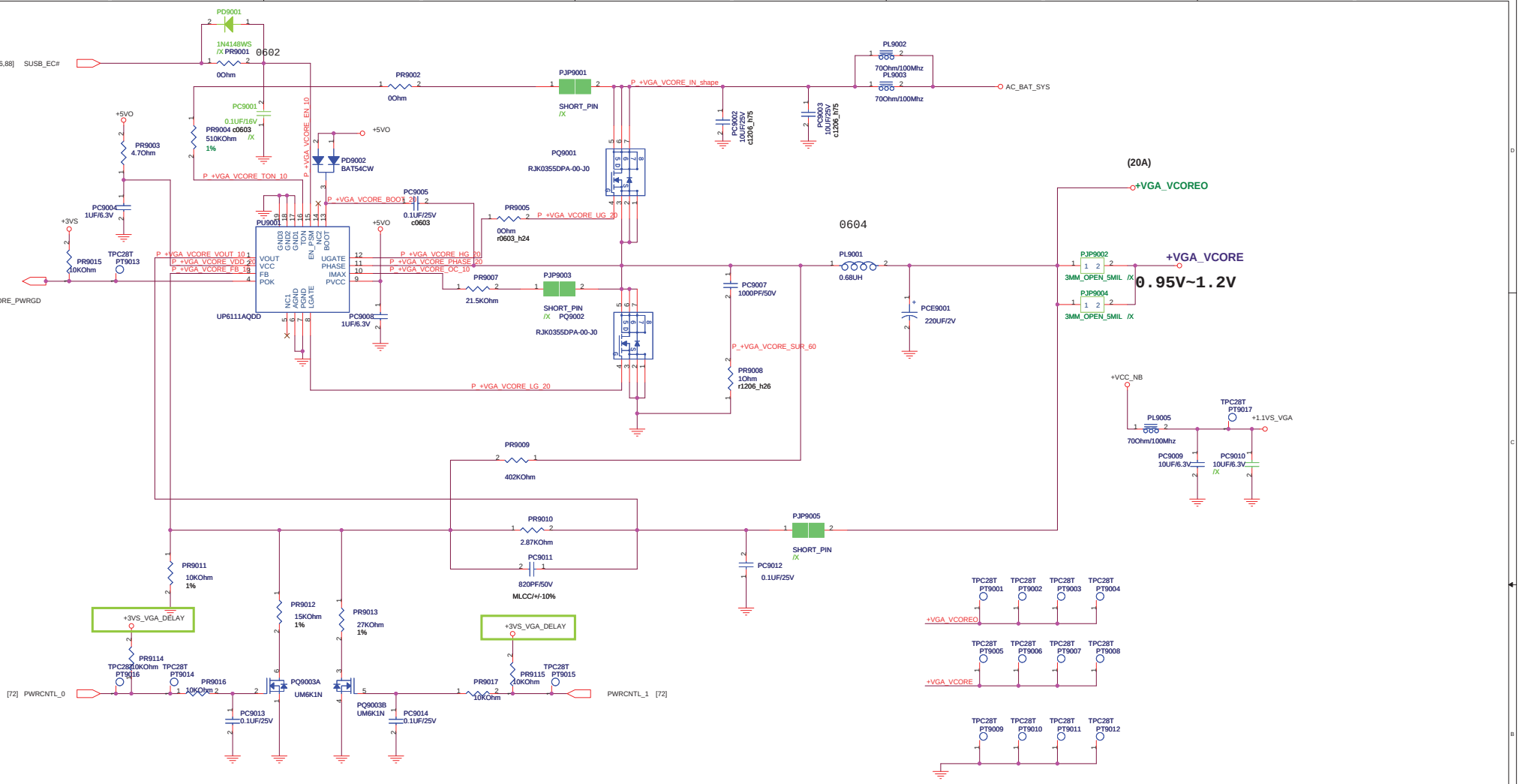
Size	Project Name	Rev
C	F83T	1.0

Date: Tuesday, May 26, 2009 Sheet 88 of 91



<Variant Name>

ASUSTek Computer INC.	Title : Power_Charger	
	Engineer: Limy_li	
Size: A3	Project Name: F83T	Rev: 2.1G
Date: Tuesday, May 26, 2009	Sheet 89 of 91	



PWRCNTL_0	PWRCNTL_1	VGA_VCORE	
0	0	0.964	-5%
0	1	1.043	Normal
1	0	1.106	+5%
1	1	1.185	+10%

Controller

1. Voltage & Current:

   +1.2VSUS: 16A

2. Frequency:

Ton=3.85p*Rt(on)/Vin-05=0.3us
Frequency=Vout/(Vin*Ton)
=500KHZ

3. OCP:

   Set PR8506=21.5kohm
   Iocp=Rocp*20/Rds(on)=26A

4. Soft start time:

   Soft-Star duration is 1.35ms

5.Inrush Current:

   C total =220uF
   I
   inrush=0.163A

Power stage

1. I/P Current:

   I in = Vo*Io/(0.75 * Vin) =0.85A

2. Ripple Current:

   Iripple=3.74A

3. Dynamic:

   Ipeak=6.1A
   ESR/2=4.5mohm
   V=27.5mohm

4. Inductor Spec:

   Isat=25A
   Idc=15.5A
   DCR=5.5mohm

5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=16.5mOhm (Vgs=4.5V)
Icont=30A (T=25)
Ipeak=120A (Pause<10us)

<Variant Name>

ASUSTeK COMPUTER INC

Title: Power_+VGA_VCORE

Engineer:

Size	Project Name	Rev
C		1.0

Date: Tuesday, May 26, 2009 Sheet 90 of 91

Date:05/19/09

1.Del PQ8012&PR8035&PC8027 in 80_Powe_charge

Date:05/21/09

1.Chagne VCORE H-S MOS PQ8101 to PH9030AL

<Variant Name>

ASUSTeK COMPUTER INC	Title : Power_History	
	Engineer:	
Size: A	Project Name	Rev: 1.0
Date: Tuesday, May 26, 2009	Sheet 91 of 91	